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# Phase Frequency Detector with Delay Cells for Achieving Low Blind and Dead Zone

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***Abstract***- A Phase Frequency Detector (PFD) with low blind and dead zone is presented in this paper. The XOR cells used as delay cells in the reset path are really appropriate for decreasing the blind and dead zone. Two extra inverters which are employed in pre-charge state are useful for preventing the short circuit. With reducing the blind zone into $36^0$, the detection range of PFD is improved significantly. The proposed PFD which is simulated in 0.18µm CMOS technology can work at 1.8V supply voltage. The maximum operating frequency of this PFD is 2GHZ, while the power dissipation is about 0.3mW. The layout of the designed PFD estimated the chip area about 3700µm$^2$.

***Keywords***- *phase frequency detector, blind zone, dead zone, delay cell, detection range.*

## I. INTRODUCTION

The advanced improvement in wireless devices leads to ameliorating designs with decreasing power consumption, chip area and cost. Most of the wireless applications in communication systems use frequency synthesizer as phase-locked loop (PLL). One of the main blocks in frequency synthesizer is PFD which detects the phase and frequency difference between the reference clock and the divider feedback signal [1, 2]. As a result of phase and frequency detection, the output of the PFD is pulses which their width shows the difference of two inputs. Two important factors that determine the characteristics of the PFD are dead zone and blind zone. A dead zone is the critical problem when two inputs have the phase difference near zero, while a blind zone happens when the phase difference reaches $\pm 2\pi$ and the PFD has problems with receiving some rising edges during the reset time [3].

In order to reduce the dead zone, the reset path is employed to the PFD to set the width of pulses at the output of the PFD when the phase difference approaches zero [4]. As the PFD pauses during the reset time, it can't work properly and a blind zone produces in the time of frequency acquisition. Therefore the detection range of PFD is affected by the blind zone. The most common technique used recently is applying a delay cell which is absolutely helpful in improving the performance of the PFD.

There are several PFD architectures which have been proposed in previous papers, such as pre-charge type PFD, ncPFD and latch- based PFD [4]. Although pre-charge type PFDs have a very high speed, they are sensitive to the phase error and have a limited detection range $(-\pi, +\pi)$ [5]. The ncPFDs, if having high speed and low dead zone, depend on the duty cycle of the input clocks. In this paper latch- based PFD with dynamic logic is used as a result of having faster operation, low power dissipation, wide detection range and low sensitivity to the input duty cycle [4, 6].

This paper is organized as follows. Section II describes the PFD operation and the techniques used for decreasing the dead zone and blind zone. The simulation results are presented in section III and finally section IV concludes the whole work.

## II. PHASE FREQUENCY DETECTOR PERFORMANCE

The proposed PFD shown in Fig. 1 consists of two extra inverters for each dynamic TSPC (True Single-Phase Clock) circuits and two XOR cells. The two inverters are used not only for prohibiting the short circuit in the PFD, but also for extending the reset path, therefore the dead zone is improved effectively [6, 7].

The operation of the PFD starts with initial states when both UP and DN signals are low [8]. In this case M1, M2, M8 and M9 are on and the voltage of the U1 and D1 nodes reaches to VDD. When the rising edge of REF signal reaches to the PFD, M6 and M7 are on and discharge the voltage of U1 node. Therefore the UP signal goes high and remains on logic high until the rising edge of FEED turns on M13 and M14 and makes the DN signal high. In this time the reset path is active and decreases the voltage level of M3, M4, M10 and M11 to zero. Therefore both UP and DN signals discharge to the low logic.

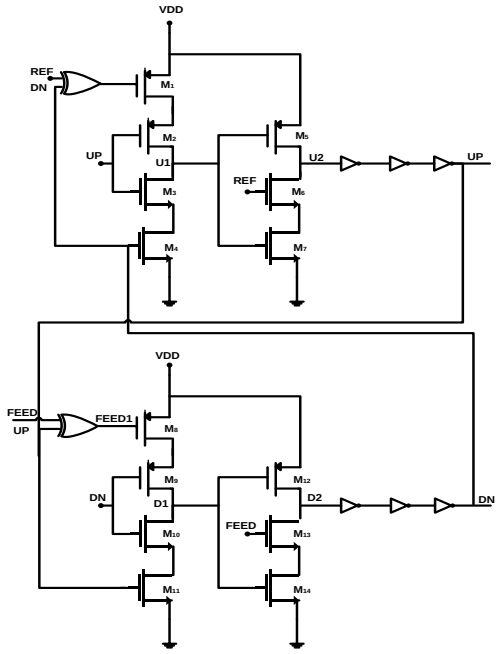


Figure 1. The proposed PFD

The most critical operation of the PFD happens when the phase difference of two inputs is near ±2π which leads to the blind zone. In recent years various techniques have been introduced and employed to the PFDs in order to create a delay in reset path which culminates in reduction of the blind zone. In [9]- [11] AND gates in reset path has been used as delay cells while in [12, 13] inverters and NAND gates provide a delay in PFD. Basically there are two methods to establish a delay for improving the detection range of PFDs. These two methods are included input pulse delay and input edge delay which has been presented in [1].

In this paper first method is used by applying the XOR gates to the input path of PFD. As each signal enters to the XOR gate with logic high contributes to the same signal. XOR gate doesn't change the input signal except providing a delay which can slightly change an input phase. As a matter of fact this weak variation in the input phase diminishes the blind zone and has an effect on extending the detection range of PFD. In Fig. 2 the schematic of the XOR gate with the equal circuit of it that consists of two NAND gates are shown. Considering the fact that NAND gates' operation is complete, they are used as one of the basic and universal gates in building the other logic gates and integrated circuits.

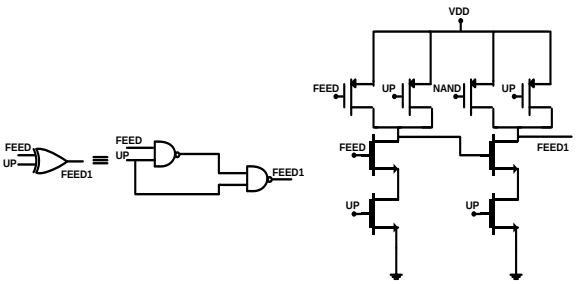


Figure 2. The XOR gate and its equal circuit

## III. Simulation Results

The aim of the designers is to invent the PFD with the minimum blind zone. When the phase difference of the two inputs is ±2π, the ideal outputs are the logic high in UP and logic low in DN, but simulation results in 0.18μm CMOS technology show the waveform of two outputs like Fig. 3. These pulses which are created in outputs produce errors in the PFD which is called blind zone. For the purpose of analyzing the operation of the PFD with XOR gates, simulation results which are presented in Fig. 3, compare two PFDs without XOR gates and with XOR gates, while two inputs have a phase difference about ±2π. As it is clear in Fig. 3(b) the duration of logic low for DN signal and logic high for the UP output is increased in the proposed PFD. The remarkable result of the simulation is the improvement in the blind zone, given the fact that the time which signals UP and DN keep at logic high and low respectively is extended.

For the calculation of the blind zone in the time domain, the width of the DN pulse which is shown by $T_{DN}$ in Fig. 3(b) should be measured [1]. This parameter in the phase domain is presented by Δ and equals to $\Delta = 2\pi \times (T_{DN} / T_{REF})$ ,where $T_{REF}$ is the period of the REF signal. If there is no XOR gate as delay cell in the PFD, the blind zone is calculated 0.34ns in the time domain which is the same as $49^0$ in the phase domain. By applying the XOR gates to the input paths of both TSPC circuits according to the Fig. 1, the blind zone in the time domain and phase domain is computed about 0.25ns and $36^0$ respectively which is stated the advanced operation of the designed PFD.

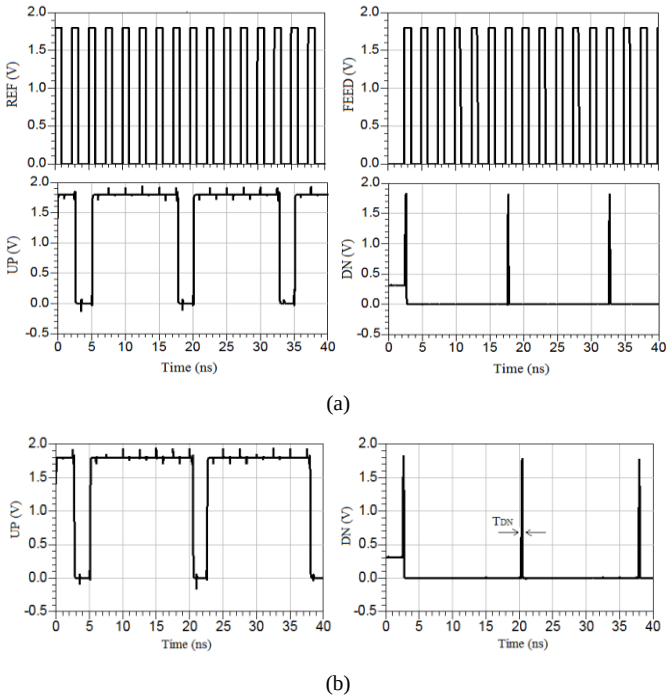


Figure 3. (a) UP and DN outputs of the PFD without delay cell in relation with REF and FEED signals. (b) UP and DN outputs of the PFD with delay cells

Another important factor which is vital for evaluation the PFD circuits is the maximum operating frequency. For the purpose of calculating the maximum operating frequency, the phase difference of two inputs should be set ±π. In this case the operating frequency is the inverse of 4 times the DN signal pulse width [6]. In the designed PFD, by providing the phase difference of two input signals about ±π, the output of DN signal is achieved as Fig. 4. Finally the maximum operating frequency can be obtained about 2GHz based on the pulse width of the DN output signal.

The proposed PFD works at 1.8V supply voltage and consumes 0.3mW power which is improved a lot in comparison with the conventional PFDs, by eliminating the static power [6].

Fig. 5 shows the layout of the designed PFD which occupies 3700µm$^2$ chip area. In order to compare the proposed circuit with the recent work TABLE I is presented. As it is obvious the power consumption and the maximum operating frequency of this work are ameliorated than the other PFD in the same technology.

## IV. CONCLUSION

In this paper, the PFD with low blind zone is presented with the XOR gates delay cells. Two extra inverters are used in order to reduce the dead zone and eliminate the static power, as preventing the short circuit. Since dead zone and blind zone are improved in this circuit, the detection range of PFD is extended while the power dissipation is diminished. The proposed PFD simulated in 0.18µm CMOS technology works at 1.8V supply voltage. Its maximum operating frequency is 2GHz while the blind zone is calculated about 36°. The layout of the designed PFD shows 3700µm$^2$ chip area and the power consumption is about 0.3mW.

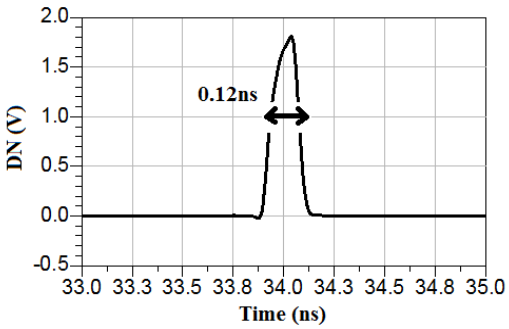


Figure 4. The pulse width of the DN output when the phase difference of the two inputs is ±π

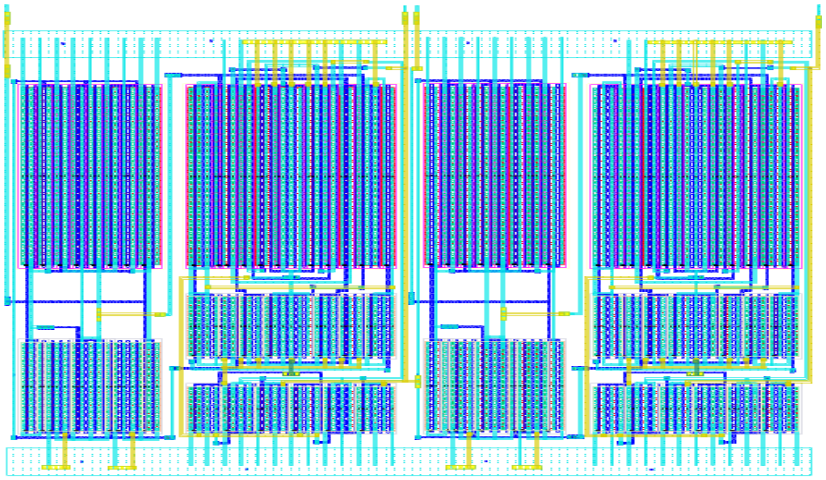

Figure 5. The layout of the proposed PFD

TABLE I. THE COMPARISON BETWEEN DESIGNED PFD AND RECENT PAPER

| | Technology (µm) | Operating Frequency (GHz) | VDD (V) | Power Consumption | Detection Range |
|---|---|---|---|---|---|
| [1] | 0.18 | 1 | 1.8 | 0.5mW | 360$^0$ |
| [2] | 0.13 | 1.5 | 1.2 | 10.5µW | 360$^0$ |
| [3] | 0.13 | 2.94 | 1.2 | 496µW | 360$^0$ |
| [7] | 0.25 | 1.53 | - | 1.4mW | 360$^0$ |
| This work | 0.18 | 2 | 1.8 | 0.3mW | 360$^0$ |

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