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A DESIGN OF DSPIC BASED SIGNAL MONITORING AND PROCESSING SYSTEM

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ABSTRACT

In this study, our objective is to develop a dsPIC based signal monitoring and processing system for analogue signals such as physiological originated signals (ECG, EMG, EEG, etc.). Microcontroller or microprocessor based monitoring systems can be much cheaper than PC based systems. However, the implementation of digital signal processing techniques using microcontroller is neither simple nor straight forward. The designed device consists of following hardware stages; a microcontroller adaptor board, dsPIC development board, (128×64) graphic LCD, and (4×4) keypad. Also, there are five different software modules which are ADC (Analog Digital Converter), FFT (Fast Fourier Transform), graphic LCD, keypad, and filter programs. The proposed device takes analogue signals via an ADC module and processes them with dsPIC by using keypad commands and then allows to plot at graphic LCD.

Keywords: Microcontroller, dsPIC, signal monitoring, signal processing, physiological signals.

1. INTRODUCTION

The term "monitoring" has been using to identify an integrated approach to data capture and analysis, decision making based upon a microcontroller or a distributed set of microcontrollers. The approach aims to locate decision making capabilities close to the source of data being considering whilst providing enhanced, real time access to the information generated [1]. Microcontroller or microprocessor based monitoring systems can be much cheaper than PC based systems. However, the

Received Date: 08.08.2008 *Accepted Date:* 05.01.2009 implementation of digital signal processing techniques using microcontroller is neither simple nor straight forward. This has been largely due to limitations in device's ability to provide the mathematical capabilities required. This situation is however changing with the evaluation of products such as dsPIC microcontrollers which are able to acquire and process the signals needed in monitoring applications. Due to the cost effectiveness of the devices, it is economically feasible to embed any required number of them within a machine or process [1]. Each device may be specially configured to act a sensing system for a particular machine element or process function.

Then, they can be linked together to form a distributed sensor network.

Digital signal processing applications seek to extract useful information from an incoming set of signals, represented by sequence of numbers. The algorithms, or computational prescriptions, for extracting this information are originally invented and developed in general-purpose computing environments in which the speed of modifying and retesting the algorithm is more important than the speed of executing the algorithm [2]. In this research computing environment, potential algorithm is first tested on small amounts of data which have been chosen or simulated to mimic certain important situations.

In a real time signal processing application, the samples of the digital signals arrive at the input of the processing system. The samples arrive over some interval of time, until a group of samples, known as a frame, have arrived that are sufficient to begin processing. Processing then begins to obtain a more information rich version of the sample data. Performing these computations on this sample requires a certain computational time.

Real time signal processing completes the computation of the output associated with a frame of input signal samples in a time that does not exceed the duration of that time [2]. In generally, for a real time application, portable implementation is necessary if that algorithm is to find practical use. The dsPIC microcontrollers can be able to implement such implementations.

In this paper, a dsPIC microcontroller based device which allows monitoring and processing of analogue signals such as physiological originated signals (ECG, EMG, EEG, etc.), is proposed. This device consists of following hardware stages; a microcontroller adaptor board, dsPIC development board, (128×64) graphic LCD, and (4×4) keypad. Also, there are five different software modules which are ADC, FFT, graphic LCD, keypad, and filter programs. The proposed device takes analogue signals via an ADC module and processes them with dsPIC by using keypad commands and then allows to plot at graphic LCD.

The manuscript is outlined as follows. In Section 2, we describe the software modules of the system. In Section 3, we introduce the hardware structure of the system. The results are presented and discussed in Section 4. Finally, Section 5 contains some concluding remarks and a proposal for further work.

2. SOFTWARE MODULES

In the system design, the speed of computation and memory capacity are considered as two most important characteristics. Since dsPIC30F6010 device has these properties, it has been chosen for our design. This chip has the following specifications;

- 30 MIPs processor speed
- 10 bit ADC
- 4 kbyte EEPROM
- 8 kbyte SRAM
- 144 kbyte program memory
- 24 bit instruction bus
- 16 bit data bus
- 1 clock cycle DSP processing
- Optimized instruction architecture with versatile addressing modes.

Microchip MPLAB v2.50 [3] is used for software modules. Then, C codes are compiled by using C30 compiler. The following submodules constructed the main software module;

- ADC program
- FFT program
- Graphic LCD program
- Keypad program
- Filter application program

2.1. ADC Program

To process the analog signals coming from some physical originated sources, those signals must be converted to the digital form via ADC. For this aim, we used a 10 bit A/D converter module [4]. The conversion speed is adjusted by SAMC (Auto-Sample Time Bits) bits which are located in ADCON3 (A/D Control Register 3). After that, the obtained 16 bits binary value is written in ADCBUFO register. The ADC timing diagram is given in Fig. 1.

Since dsPIC signal processing function were written with signal fractional numerical format,

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we have used this format for all signal processing functions that we developed. For some applications, we have formed signal sequence with different lengths. For example, the FFT calculation uses a sequence with 512 samples.

2.2. FFT Program

In order to adjust FFT length, FFT_BLOCK_ LENGTH and LOG_BLOCK_LENGTH coefficient must be defined in "parameter.h" user defined library. This module can be able to calculate a FFT process with 64, 128, 256, and 512 sample lengths. FFT processing can be implemented as following way [5, 6] and DSP processing cycles are given in Table 1.

- Initialization: Twiddle factor coefficients are defined.
- Input signal is scaled to be located at [-0.5 0.5] interval.
- Butterfly computation is implemented by calling "FFTComplexIP ()" function from Microchip signal processing library.
- Bit-reversed RE_ordering is a part of FFT algorithm. In this routine, FFT sequence is reordered in bit-reversed manner.
- Square Magnitude computation of each complex entity of FFT outputs.
- The peak value searching is implemented by "vector max ()" function.

2.3. Graphic LCD Program

The all functions that are needed for plotting of provided sequence are written in "GLCD.c" source file which including following keys; starting, character print, inserting of a dot, and plotting. LCD interface is given in Fig. 2. Figure 1. ADC timing diagram.

2.4. Keypad Program

This module detects keystrokes via an interrupt function which includes "key_find ()" function. In order to detect any key, for each key, we used a specific key name in "parameter.h" user defined library.

2.5. Filter Program

The one of the most important property of proposed device is to filter analog signals in realtime digital filtering manner. The filters used can be designed by "Digital Filter Design Tool" of Microchip Coorparation. For practical purpose, we design FIR and IIR filter structures [7]. For a low-pass filter, the following parameters were defined; cut-off frequency, pass-band ripple, stop-band ripple, and length of filter coefficients. We also formed MPLAB C30 compatible assembly file which can be inserted to other source files.

3. HARDWARE CONSIDERATIONS

The proposed system consists of the following hardware components: 1) Microcontroller adaptor card, 2) dsPIC control card, 3) Graphic LCD, 4) Keypad, 5) Power supply, 6) Processor programming connector. These modules have been described above and given as Fig. 3.



Cycle Count Equation	Conditions*	Number of Cycles	Execution Time @30 MIPS
—	N=64	3739	124.6 µs
—	N=128	8485	282.8 µs
—	N=256	19055	635.2 µs
—	—	1	33 ns
53+N(4+M)	N=32, M=32	1205	40.2 µs
41+N(4+7M)	N=32, M=32	7337	244.6 µs
36+N(8+7S)	N=32, S=4	1188	39.6 µs
46+N(16+7M)	N=32, M=8	2350	78.3 µs
20+3(C*R)	C=8, R=8	212	7.1 µs
16+C(6+3(R-1))	C=8, R=8	232	7.7 µs
17+3N	N=32	113	3.8 µs
19+7(N-2)	N=32	229	7.6 µs
17+4N	N=32	145	4.8 µs
16+2N	N=32	80	2.7 µs
—	—	7	231 ns
*C= #columns, N=# samples, M=#taps, S=#sections, R=#rows **Complex FFT routine inherently prevents overflow			
	Cycle Count Equation 	Cycle Count Equation Conditions* — N=64 — N=128 — N=256 — N=256 — — 53+N(4+M) N=32, M=32 41+N(4+7M) N=32, M=32 36+N(8+7S) N=32, S=4 46+N(16+7M) N=32, S=4 20+3(C*R) C=8, R=8 16+C(6+3(R-1)) C=8, R=8 17+3N N=32 19+7(N-2) N=32 16+2N N=32	Cycle Count Equation Conditions* Number of Cycles — N=64 3739 — N=128 8485 — N=256 19055 — N=256 19055 — — 1 53+N(4+M) N=32, M=32 1205 41+N(4+7M) N=32, M=32 7337 36+N(8+7S) N=32, S=4 1188 46+N(16+7M) N=32, M=8 2350 20+3(C*R) C=8, R=8 212 16+C(6+3(R-1)) C=8, R=8 232 17+3N N=32 113 19+7(N-2) N=32 229 17+4N N=32 80 — — 7 mples, M=#taps, S=#sections, R=#rows inherently prevents overflow To any float

Figure 2. LCD interface. Table 1. DSP processing cycles.

The microcontroller (dsPIC 30F6010) has thin quad flat packet pin configuration [8]. In order to easy assemble it, we designed an adaptor card. To operate dsPIC 30F6010 microcontroller and LCD graphic display, it is needed to use 5 V power supply. For this aim, 7805 based power module (5 V – 0.5 A) is designed. Further, Microchip MPLAB ICD2 module is used for microcontroller programming. The communications of both components are provided via RJ11 socket.



4. RESULTS

In this section, some program outputs will be given. First, we have considered the plotting of the signals. For this aim, the following procedure should be employed.

- Select signal plotting process on signal menu,
- Enter the suitable off-set value and user defined sampling rate.

In the Fig. 4, a sinusoidal signal plotting is given. A typical FFT output of a sinusoidal signal with 600 Hz sampling frequency is given in Fig. 5.

Finally, we have implemented digital filter application with "Digital Filter Design Tool" developed by Microchip Coorperation. Finite Impulse Response (FIR) and Infinite Impulse

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Figure 3. Hardware structure of the proposed system.



(a)



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Figure 5. The FFT output plotting.

First, the following filter parameters; cut-off frequency, pass-band ripple, stop-band ripple, and the length of filter coefficients should be entered. After that, the structure of designed filter will be given graphically. MPLAB C30 compatible assembly file should be formed, as well. In Fig. 6, a low-pass filter design outputs are given (for 1 kHz sampling rate). Then, the constructed assembly file is inserted to program. For filtering any signal coming from ADC unit, the signal length and sampling rate should be selected via filter menu. Finally, a square wave analog signal with 1 kHz fundamental frequency and 10 kHz sampling rate is filtered by the designed low-pass filter (cut-off frequency is 1.2 kHz). The filtered output is given in Fig. 7.

5. CONCLUSIONS

In this paper, the authors have described a dsPIC microcontroller based system for the monitoring and processing of the analog signals. The system is able to separately display the signal itself and its FFT output. In addition, we are capable of running any FIR and IIR filter defined previously by "Digital Filter Design Tool" of Microchip Coorperation. Besides using for any analog signal, the device could be used as physiological based signal monitor for biomedical applications. Also, it can be served as a portable spectrum analyzer in limited frequency interval.

Future developments of the proposed monitoring system are to consist in replacing the more miniaturized version characterized by [7] maximum memories have to be employed.

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microelectronics are his interested fields.

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Figure 7. The filtering of an analog square wave signal.

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Figure 6. The low-pass filter design outputs.

processing, biomedical circuit design, artificial circulation system, modeling and microprocessor applications.

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