Designing and constructing PFC converter by boundary layer control (BLC) in order to correct power factor and harmonic migration

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Abstract. Rectification can be easily done by using rectifier circuits such as Diode Bridge and a relatively large capacitor in order to provide DC electricity. This results in power coefficient reduction and harmonic distortion increase .To cope with such problems, using PFC converter between Diode Bridge and capacitor filter leads to the fact that sinusoidal current which has the same voltage with input voltage is taken from the supplier. This paper studied designing, modeling, and simulation using Pspice software .Constructing a prototype and using Boost converter, the efficiency of 93.26 percent was reported in voltage of 222 and THD was obtained for lower than 8.5 percent for voltage range of 85-256.

Keywords: Boost, Power factor correction, PFC, harmonic migration, THD

1.   INTRODUCTION

In the last few years, as a result of increased popularity of DC-DC converters due to higher efficiency, a considerable number of improvements happened due to the ability to increase circuit frequency and smaller converters in comparison with AC-AC converters. The only problem of DC-DC converters is DC inaccessibility in most locations, leading to limited usage of these converters. Eventually, rectification is obliged in order to use such converters in off-line connected applications or generally in locations with AC. Common converters used in AC connected applications usually take advantage of full wave rectifier with a large capacitor in order to reduce voltage ripple. This issue destroys input waveform and it will lead to harmonic increase [1]. Fig.1 shows input voltage rectifier circuit along with input voltage and current forms.
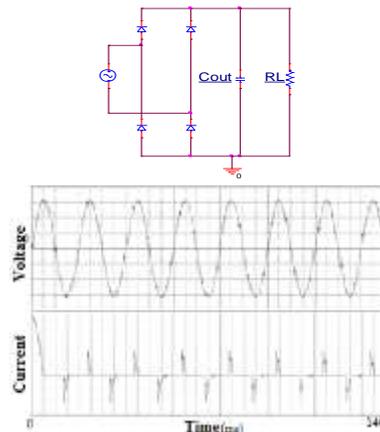
Figure 1. Voltage rectifier along with input voltage and current waveforms.

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Such circuits have some disadvantages such as electricity-taking increase of peak and effective current from power supply, AC voltage destruction, and additional voltage in neutral wire of three-phase systems, and weak exploitation from energy of power systems.

To cope mentioned problems, using PFC converter between diode bridge and capacitor filter leads to the fact that a sinusoidal current which has the same voltage with input voltage in taken from power supply. [2, 3]. Power factor in these types of converters is close to unit and the mentioned problems are met. Fig. 2 shows converter with PFC. Nevertheless, FlyBack, Cuk, or Sepic topologies can be used to implement Power Factor Correction (PFC) circuit [4-7]. This paper focuses on these types of converters due to greater number of advantages of PFC boost circuit and more applied usages. The following merits are mentioned as the main reason of implementing PFC circuit on boost circuit:

Switch source is linked to the ground thus switch drive is easier.

Basically, boost circuit is located between Diode Bridge and switch, therefore, it leads to reduced $\frac{di}{dt}$ and noise and the necessity to use EMI filter [8].

Basically, the circuit needs less additional elements, thus, it is cost effective.

Although PFC boost converters are the most popular converters as a result of mentioned advantages, these converters has some drawbacks:

1- High starting current due to large output capacitor.
2- Lack of current limiter during additional load and in short circuit condition due to direct link between line and load [9].
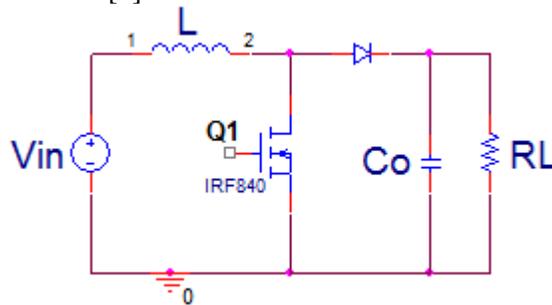
Figure 2. Boost converter.

Power factor correction can be done through various methods of PFC boost converter control such as current peak, average-current control, hysteresis control, PWM control of discrete current performance mode, and boundary control. [10].

Some advantages are reported for current peak [10]: 1. Switch current must only be measured which can be done by current transformer, thus, measuring resistance loss will not exist. 2. Current fault amplifier and compensation network are not needed. 3. The possibility of limiting switch current. Disadvantages of this method [10]: creating harmonic oscillation in in higher-than-50% duty cycles, thus, slope compensator is needed. 2. Despite the presence of slope compensator, in case of increased line voltage and during low load, input current distortion will increase [11]. 3. Higher sensitivity.

Some advantages of average current control method are as following: 1. No need to slow compensator 2. Controlling is less sensitive to telecommunication noise due to less current filter 3. Better waveform in comparison with peak current control method. Some disadvantages are reported:

1. Self-current must be measured. 2. Current fault amplifier is needed and various working points of converter need to be considered in one line cycle while designing compensator network.

Despite previous two methods, hysteresis control method works based on varying frequency. Unnecessary external ramp is considered the merit of this method compared to peak current control method. [10].

PWM control method of discrete current performance mode is used in Sepic, Cuk, and Fluback topologies; however, this controlling method creates harmonics in lines in Boost topology. In this method, internal current loop is removed [10].

In boundary layer controlling method, the on-switch duration remains unchanged during a line frequency cycle and switch turns on when it reaches to zero self-current. Thus, converter acts on the boundary between continuous conduction mode and non-continuous conduction mode. In this method, switch turns on in current of zero, therefore, loss declines. On the other hand, conduction loss and component stress rise by increased peak current and stronger filter might be needed [10]. This controlling method is an especial condition of hysteresis control method. General plan of this control is shown in Fig. 3. Sudden input current is made up of in-row triangular currents where their summits are in accordance with line voltage. Thus, input current average is also in accordance with line voltage during one duty cycle. This feature is the highlighted characteristics of this controlling method as automatic-forming current [10].

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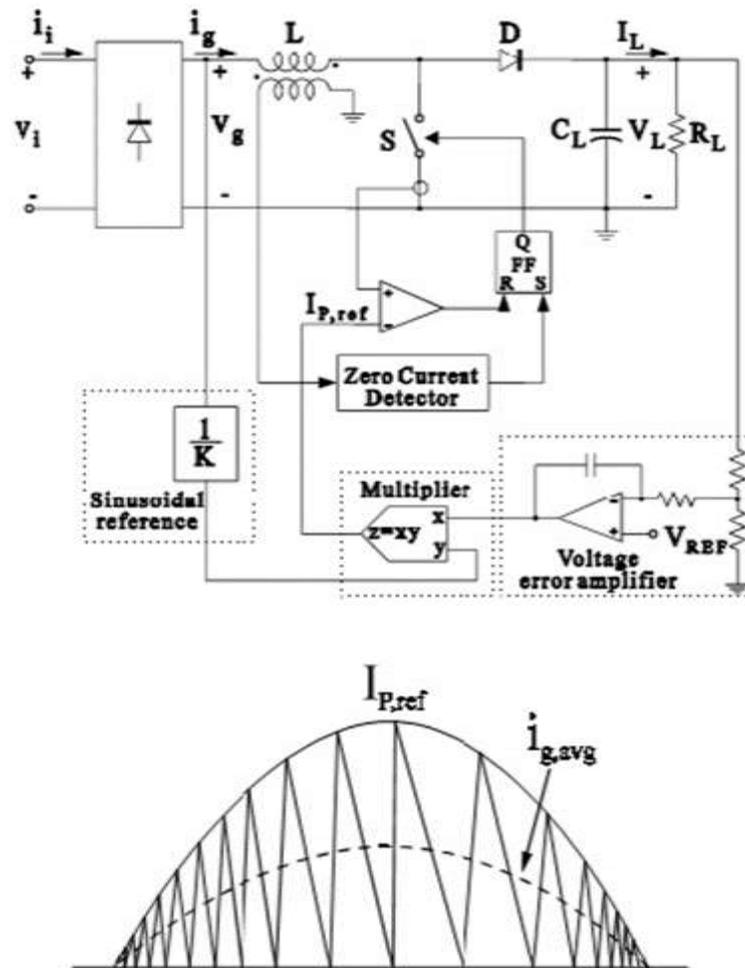

Figure 3. Boundary control method.

PFC is studied in the next section by applying boost converter in transition mode. Finally, simulation results are provided by Pspice software.

2. DESIGNING 80-WATT PFC BOOST CONVERTER CIRCUIT BY BOUNDARY LAYER METHOD

To design values of this converter, equations in [12] are used. Designing specifications are listed in table (1) to reach the objective of study.

Table 1. Specifications of designing boost PFC converter.

Parameter	Definition	Values
$V_{irms(\min)} - V_{irms(\max)}$	Input voltage range (AC)	85-265 [v]
V_o	Regulated output voltage(DC)	400[v]
P_o	Output power	80[w]
f_{sw}	Minimum switching frequency	$f_{sw(\min)} = 20\ [kHz]$
ΔV_o	Maximum ripple output voltage	$\Delta V_o \leq \pm 10\,V$
ΔV_{ovp}	Maximum additional output voltage	40 [V]
η	Expected efficiency	$\eta > 90\%$
$P_i = \dfrac{P_o}{\eta}$	Input power	88.89 [w]
$I_o = \dfrac{P_o}{V_o}$	Output current	.2 [A]
l_{gap}	Core gap distance	1.25 [mm]
A_e	Effective surface of core	118 [mm^2]

2.1 Designing power section

2.1.1 Diode Bridge

To consider Diode Bridge, consideration must be given to effective input values, maximum peak of line voltage, and heat information.

$$I_{rms} = \frac{P_i}{V_{rms(\min)}} = \frac{88.89}{85} = 1.05\ [A] \qquad (1)$$

2.1.2 Input capacitor

Filter capacitor of above frequency must weaken switching noise due to high frequency self-current ripple. The worst condition will happen in minimum peak of input voltage. Maximum ripple of high frequency voltage ripple is usually considered between 1 to 10 percent of minimum input voltage determined by r coefficient

$$(2)$$

$$C_{in} = \frac{I_{rms}}{2\pi.f_{sw}.r.V_{irms(\min)}} = 1\mu F$$

2.1.3 Output capacitor

Selecting output capacitor depends on output voltage and considered additional voltage, output power, and acceptable voltage ripple. Voltage ripple is 100 to 200 hertz (two times as many as main frequency) of capacitor impedance and capacitor current peak

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$$C_o \geq \frac{I_o}{4\pi.f.\Delta V_o} = \frac{P_o}{4\pi.f.V_o.\Delta V_o} = 47\mu F \quad (3)$$

2.1.4 Self boost

First, inductance value must be determined.

$$L = \frac{V_{irms}^2.(V_o - \sqrt{2}.V_{irms})}{2.f_{sw(min)}.P_i.V_o} = 0.8mH \quad (4)$$

where V_{irms} is minimum value. Considering the transformer core which is E25x13x7 core,3C85 ferrite, the next step is determining the number of turns of the coil,

$$\sqrt{\frac{0.8\times10^{-3}\times1.25\times10^{-3}}{\mu_0\times118\times10^{-6}}} \approx 82 \text{ turn} \quad (5)$$

2.1.5 Selecting Poswer Mosfet

The important question is selecting R_{DSon} Mosfet which depends on output power, additional sum of regulated voltage, and security margin. Distribution system of Mosfet power depends on switching loss and conduction. According to the Mosfet switches in Markets, we selected IRF840 switch to reach the most ideal condition.

2.1.6 Boost diode

Boost diode is a Fast Recovery Diode (FRD) and the DC current is defined as following:

$$I_{DC} = I_o \quad (6)$$

To select diode from MUR diodes, a voltage compatible diode was selected. We used MUR880 diode for proposed converter.

2.2 Determination of current sense resistance R_s

Considering 3 voltages for $V_{MULTPKmax}$ in the following equation, we will have:

$$V_{MULTPKmin} = V_{MULTPKmax} * \frac{V_{irms(min)}}{V_{irms(max)}} = 3 * \frac{85}{265} = .96 \quad (7)$$

$$V_{XCSPK} = 1.65 * V_{MULTPKmin} = 1.58 \quad (8)$$

$$(9)$$

$$I_{R_SPK} = 2\sqrt{2} * I_{rms} = 2.94$$

$$(10)$$

$$R_s \leq \frac{V_{XCSPK}}{I_{R_SPK}} \leq .54$$

We considered the resistance of 0.2 ohm for R_s. Considering all above mentioned issues and resistive load of 2 Kilo-Ohm, we did the simulation.

3-SIMULATION AND CONSTRUCTION

Simulated converter by Pspice software is shown in Fig.4. Control circuit, input circuit waves, and output circuit waves are shown in Fig.5, Fig.6, and Fig.7, respectively. To implement Boost PFC converter, L6561 chips of ST Company were used. Constructed converter sample, its input waves, and output waves of constructed circuit are shown in Fig. 8, Fig. 9, and Fig.10. Finally, simulation results are listed in table (2) and practical results are in table (3).
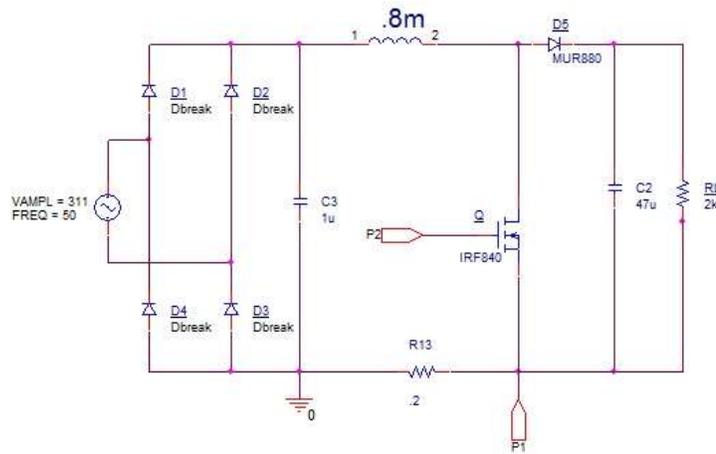

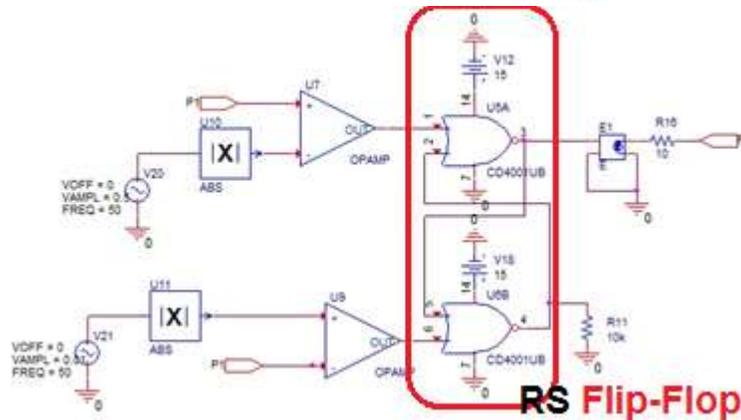Boost PFC circuit   Fig. 4:

Figure 5. Boost PFC converter control circuit.

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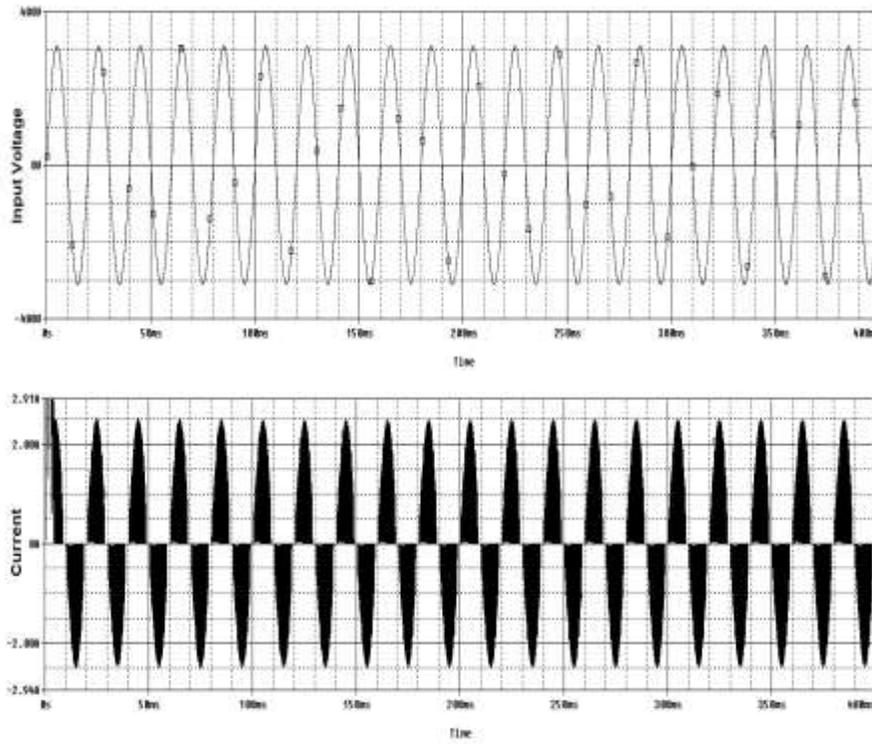

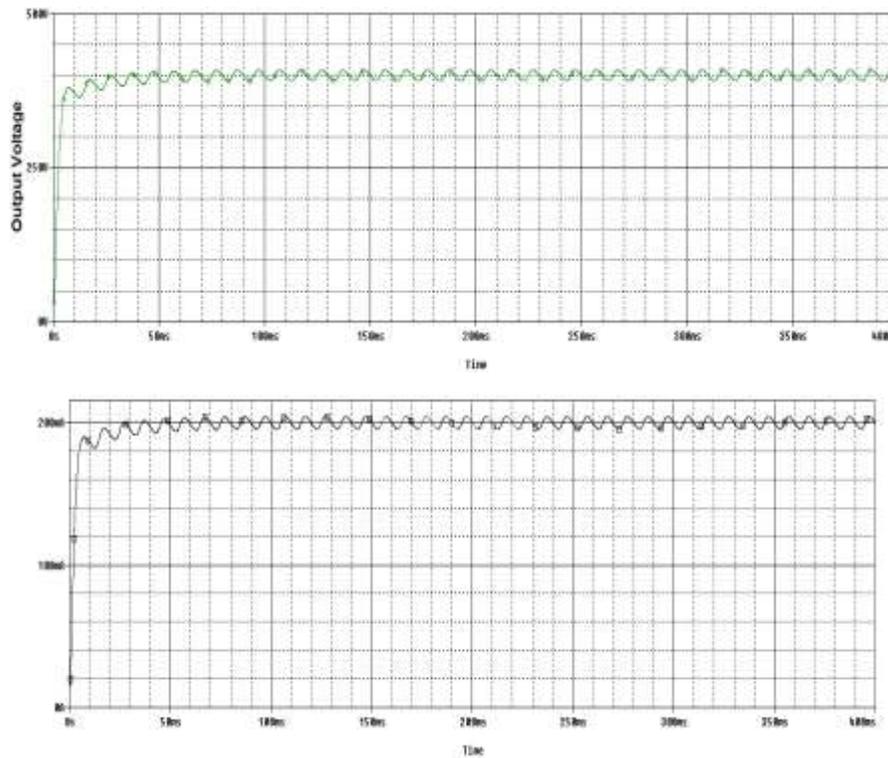**Figure 6.** Forms of voltage waves and input current.

Figure 7. Voltage waves and output current.

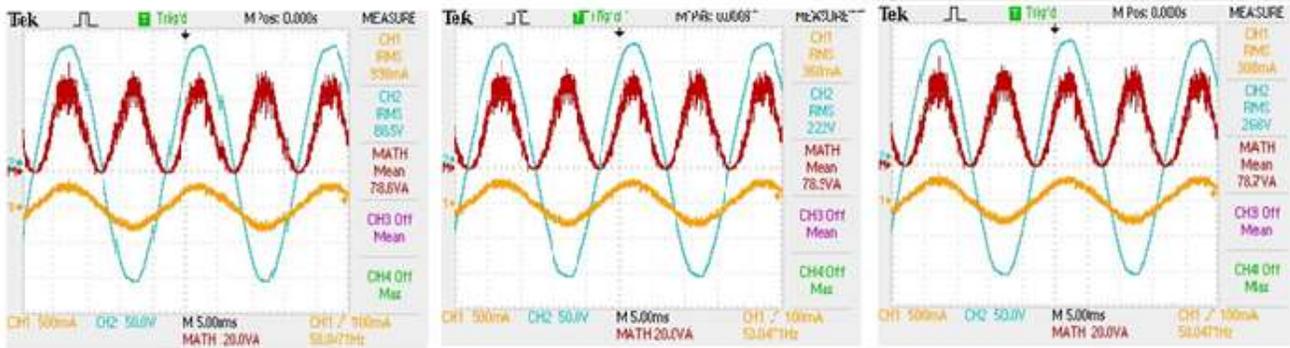**Figure 8.** Sample of Boost PFC converter.

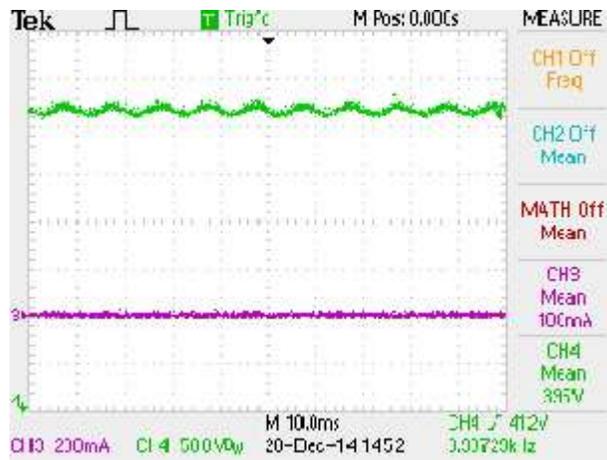**Figure 9.** Voltage, current, and input power wave forms.

Figure 10. Voltage and output current wave forms.

In order to calculate power factor, efficiency, and THD in simulation, the following equations can be used.

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$$PF = \frac{AVG(P_i)}{AVG(V_{irms} * I_{irms})} \qquad (11)$$

$$\text{Efficiency} = \frac{AVG(P_o)}{AVG(P_i)} * 100 \qquad (12)$$

$$PF = \frac{1}{\sqrt{1 + THD^2}} \qquad (13)$$

To calculate power factor, the following equation is practically used:

$$\text{Efficiency} = \frac{V_o * I_o}{P_{in}} * 100 \qquad (14)$$

As it can be seen, output voltage ripple is 10 volt which is acceptable.

Table 2. Simulation results.

THD	Efficiency(%)	PF	$P_{out}(W)$	$P_{in}(W)$	$V_{in}(V_{AC})$
6.3	91.95	0.998	80	87	85
9.6	95.24	0.957	80	84	220
18.1	96.38	0.92	80	83	265

Table 3. Practical results.

THD	Efficiency(%)	PF	$P_{out}(W)$	$P_{in}(W)$	$V_{in}(V_{AC})$
2	93	0.99	73.098	78.6	85.5
6.2	93.26	0.97	73.6	78.9	222
8.5	96	0.96	75.55	78.7	266

4.   CONCLUSION

In this article, we reached high power factor and efficiency as well as low THD for input current in a wide range of input voltage using Boost converter in transition mode. The results for 2 Kilo-Ohm is 80 Watt. Comparing the results with results of other PFC converters, we realize that proposed circuit has far less loss compared to other converters.

5.   OPEN PROBLEMS

5.1 What measures need to be taken if efficiency and power factor are not decreased in case of load charges?

5.2 Using PI controller for PFC objective using LNK403-409eg. Chips.

6. ACKNOWLEDGMENT

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