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# Low-power, Dynamic, D-type Flip-Flops for Biomedical Implant Devices

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**Abstract.** A dynamic, single-edge-triggered D-type flip-flop (SETDFF) is evaluated for implementation of a successive approximation register analog-to-digital converter intended for biomedical implant devices. The performance of the dynamic SETDFF in a 90nm CMOS technology has been compared to that of a static D-type SETDFF topology employing master-slave latches based on SPICE simulations. Both flip-flop types have been designed and implemented in a 2µm CMOS technology and their performance has been characterized. Compared with the static flip-flop implemented with master-slave latches, the dynamic flip-flop consumes less power, employs a smaller number of transistors and is capable of operating at slightly higher speeds. A dual-edge-triggered flip-flop topology based on the given dynamic flip-flop architecture is proposed in order to further reduce power consumption.

**Keywords:** CMOS, D-type flip-flop, Dynamic, low power

## 1. INTRODUCTION

Power consumption is of major concern in battery-powered electronic systems employed in implantable medical devices. Enhancing the battery life necessitates use of low-voltage and low-power circuit techniques to implement the system building blocks. Pacemakers and cardiac defibrillators represent examples of implantable devices in which analog and digital circuit blocks with ultra low power consumption are critical. Artificial pacemakers, in particular, depend on non-rechargeable batteries to sustain a lifetime of up to 10 years. One of the critical blocks in the artificial pacemaker in terms of power consumption is the analog-to-digital converter (ADC). Given the additional requirements of moderate resolution and low sampling frequency for the ADC, a successive approximation register (SAR) ADC represents an appropriate option for implementation of the implantable pacemaker, since its simple structure leads to low power consumption. A significant portion of the overall power consumption in an SAR ADC is dissipated by the flip-flops within the SAR control logic implementing the binary search algorithm. According to the approach proposed by Rossi [1], in an N-bit SAR ADC, implementation of the SAR control logic requires N flip-flops.

Flip-flops (FFs) are critical timing elements in sequential digital circuits. Along with the clock distribution network FFs allow implementation of the clocking scheme responsible for timing in a given system. Since the power consumed by the clock system represents a significant portion of the total power dissipation [2], reducing the power consumed by the flip-flops is critical in low-power VLSI system design. Furthermore, inasmuch as dynamic power is proportional to the square of the logic swing, scaling the supply voltage is the most effective approach to reduce the power consumed by the FFs. Nevertheless, scaling of CMOS circuits is accompanied by threshold voltage scaling, which leads to an exponential increase in subthreshold conduction, thereby dramatically increasing static power consumption [3]. Aside from supply voltage scaling, the power consumed by the FF can also be decreased by reducing the loading capacitance. In order to reduce the clock loading, the number of clocked transistors employed in the FF has to be reduced. To this end, dynamic FFs can be employed in which, instead of using latches as memory

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elements, memory is realized by utilizing the storage of charge on an internal node of the FF circuit. In addition, use of double-edge-triggered flip flops (DETFFs) can ideally reduce the power consumed by the clock distribution network by one-half, while maintaining the rate of data processing [4]. Alternatively, by using DETFFs the rate of data processing can be doubled at a given rate of energy consumption [5]. Therefore, double-edge clocking can either enhance the speed of operation or reduce the power consumption by the clock system.

**A dynamic SETDFF**

Employing a true single phase clock (i.e. a clock which is never inverted) has been proposed for high speed applications [6]. This SETDFF also offers the advantages of simple clock distribution and reduced area for clock lines, and alleviates clock skew problems. The true-single-phase-clock (TSPC) dynamic SETDFF employs a total of ten transistors, out of which only four are clocked. Therefore, the TSPC dynamic SETFF is potentially suitable for low-power applications due to the diminished clock load. In this work the performance of the TSPC dynamic SETDFF is compared with that of a static SETDFF based on design and implementation of both flip-flop types in a 2μm CMOS technology. Furthermore, the performance of the TSPC dynamic SETDFF has been compared with that of the static SETDFF in a 90nm CMOS technology based on SPICE simulations. Finally, a dual-edge-triggered flip-flop topology based on the given dynamic SETDFF architecture is proposed in order to further reduce the power consumption associated with the flip-flops employed in the SAR ADC intended for biomedical implant devices.

**Design AND Characterization of the Dynamic and the Static SETDFF**

**TSPC Dynamic SETDFF**

The schematic of the dynamic SETDFF circuit is shown in Fig. 1. A high-to-low clock transition causes the input to propagate to node N2 or N3 depending on the state of the input. Then, the following low-to-high clock transition causes the input stored at node N2 or N3 to propagate to the output.

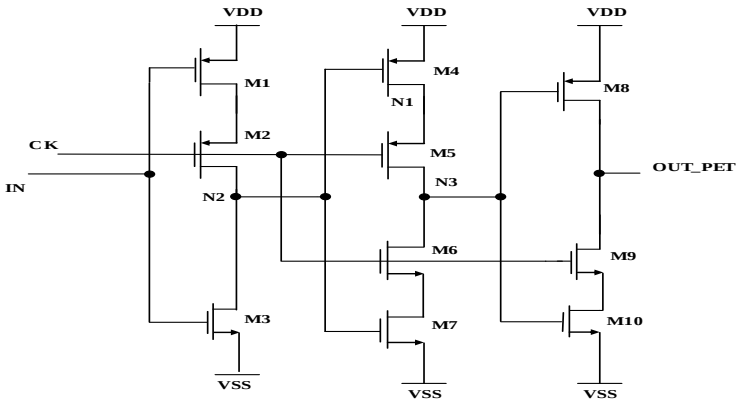


**Figure 1.** Schematic of the dynamic positive-edge-triggered DFF circuit.

At the clock transition from high to low, a low input forces node N2 to go high, since both M1 and M2 will be conducting. A high input, on the other hand, turns M3 on forcing N2 to go low. Therefore, at the high-to-low clock transition a high input signal propagates from the input and N2 to N3, since both M4 and M5 will be conducting, forcing N3 to go high.

At the clock transition from low to high, an originally low input data propagates to node N3, since both M6 and M7 will be conducting (as noted above with a low input a high-to-low clock transition forces N2 to go high). With N3 in a low logical state the output will go high, since M8 is conducting. Therefore, during the low-to-high clock transition a low input propagates in inverted form as a high state from N2 to the output. On the other hand, an originally high input

causes the output to go low during the low-to-high clock transition. This is due to the fact that a high input propagates to node N3 at the high-to-low clock transition. Accordingly, with the low-to-high clock transition both M9 and M10 will be conducting forcing the output to go low. When the clock is low the output cannot change, and when the clock is high a change in the input cannot propagate to the output. The TSPC dynamic SETDFF of Fig. 1 is, therefore, equivalent to a positive edge-triggered, inverting D-type flip flop.

The TSPC dynamic SETDFF circuit was designed for fabrication in a 2μm p-well CMOS technology with the minimum feature size used for all channel lengths. In addition, transistor widths of low to moderate size were used to achieve a compact layout. The ratios of channel width to channel length (*W/L*) were chosen such that equal rise and fall times would result assuming that the surface mobility of electrons in the n-channel transistors was twice that of holes in the p-channel transistors.

**Static SETDFF**

The static SETDFF is implemented using standard master and slave latches as shown in Fig. 2.

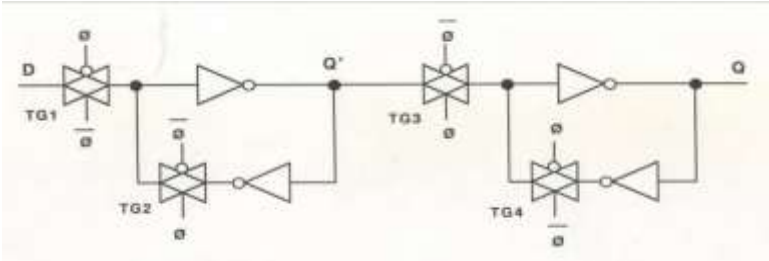


**Figure 2.** Standard static master-slave SETDFF.

Each latch consists of two cross-coupled standard CMOS inverters with a transmission gate inserted in the feedback loop. This implementation requires two clock signals $\varphi$ and $\overline{\varphi}$, and is equivalent to a positive, edge-triggered, non-inverting D flip-flop. A transmission gate TG1connects the D input to the master latch, and another, TG3 connects the output of the master latch to the input of the slave latch. The transmission gates allow operation as an edge-triggered D flip-flop. When the clock signal $\varphi$ is low, TG1 and TG4 are in the on state, while the TG2 and TG3 are in the off state. Therefore, the slave is isolated from the master and the feedback loop of the slave latch is closed, thereby allowing retention of the previous state. On the other hand, the feedback loop of the master latch is open and the output of the master latch, $Q'$ is the complement of the D input. During the low-to-high transition of $\varphi$, TG1 and TG4 turn off, while the TG2 and TG3 turn on. Therefore, the master latch becomes isolated from the input and its feedback loop will be closed. As a result, its output, $Q'$ adopts the complement of the D input value applied just prior to the low-to-high $\varphi$ transition. Meanwhile, the feedback loop of the slave latch is opened and its output, Q adopts the complement of $Q'$.

Sizing of transistors in the D flip-flop circuit with master and slave latches was performed based on the same considerations outlined in section IIA. In particular, the *W/L* ratios were chosen so as to obtain roughly equal rise and fall times by choosing the width of the p-channel transistor to be twice that of n-channel transistor. The $\overline{\varphi}$ clock was generated from the $\varphi$ clock signal using a balanced inverter.

**Characterization of DFF's in 2µm CMOS**

The test circuit for characterization of the DFF's consisted of the given DFF driving an identical load (i.e. fan-out of one), which corresponds to the application of the FF in a digital delay line. The DFF's were characterized only with regard to their speed performance, by examining their output waveform in relation to the input and clock signals using an input signal (D) frequency equal to one-half of the clock frequency. The waveforms corresponding to the TSPC dynamic and the static SETDFF's are shown in Fig. 3 and Fig. 4 respectively. The maximum frequency of operation, $f_{max}$ was measured for each FF by determining the maximum clock frequency for which a correct output state was obtained. Accordingly, $f_{max}$ was determined to be in excess of 250MHz for the TSPC dynamic SETDFF and 154MHz for the static flip-flop employing master and slave latches.

**SPICE Simulations**

In order to compare the speed and power performance of the dynamic versus static implementation of the flip-flops, the TSPC dynamic SETDFF and the static SETDFF circuits were designed in a 90nm CMOS technology based on the same methodology as described in section II. A negative-edge-triggered D-type flip-flop (NETDFF) was used in SPICE simulations of the dynamic flip-flop. The NETDFF, whose schematic is shown in Fig. 5, is derived from the positive-edge-triggered dynamic SETDFF of

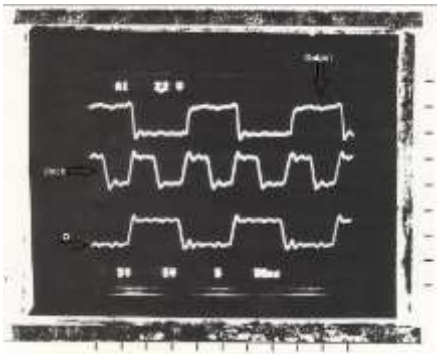

**Figure 3.** Positive-edge-triggered, Inverting TSPC Dynamic FF Waveforms in 2µm CMOS.

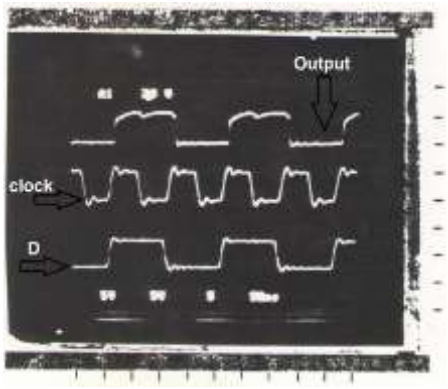


**Figure 4.** Standard Positive-edge-triggered, Non-inverting Static FF Waveforms in 2µm CMOS.

Fig.1, and is intended for implementation of a DETFF based on the TSPC dynamic approach. The waveforms demonstrating the functionality of the negative-edge-triggered TSPC dynamic and the static flip-flops in response to a pseudorandom bit sequence representing the D input are shown in Fig. 6, and Fig. 7 respectively. HSPICE simulations indicated that both topologies were able

to operate at a clock frequency of 10GHz. The waveforms corresponding to the operation of the TSPC dynamic and the static flip-flop at 10GHz are presented in Fig. 8, and Fig. 9. The TSPC flip-flop, however, exhibited a slightly lower average Clock-to-Q delay as specified in Table I. In addition, the SPICE simulations revealed that the TSPC dynamic SETDFF consumes a considerably less amount of power as noted in Table I. This is presumably due to the diminished clock load, resulting from use of only four clocked transistors in the dynamic topology as pointed out above. Furthermore, as indicated in Table I, the power-delay product of the TSPC dynamic SETDFF is more than one order of magnitude smaller than that of the static SETDFF. Therefore, the performance of the TSPC dynamic SETDFF surpasses that of the static flip-flop with regard to both power and power delay product.

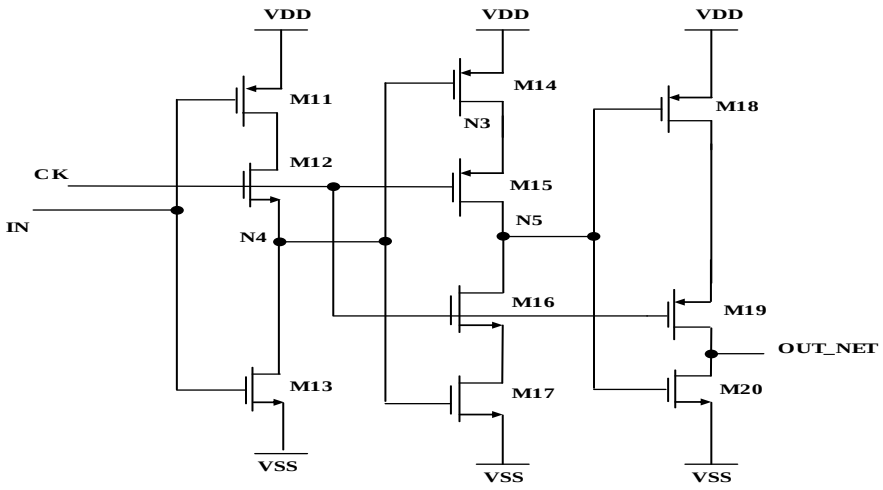


**Figure 5.** Schematic of the dynamic negative-edge-triggered DFF circuit.

**Table I.** Simulated Performance of DFFs in 90nm CMOS.

$V_{DD}$ =1V, $T$=300K, $C_L$=0.155pF, Typical Process Corner

| Design Title | Average Clock-to-Q Delay (psec) | Total Average Power ($\mu$W) | PDP (fJ) |
|---|---|---|---|
| TSPC Dynamic SETDFF | 400 | 7.57 | 3.04 |
| Standard Static SETDFF | 450 | 91.4 | 41.1 |

**Dual-Edge-Triggered Dynamic Flip-flop**

Given the relatively small amount of power consumed by the TSPC dynamic SETDFF, implementation of a DETFF based on the TSPC dynamic approach can potentially lead to a significant reduction in the power required at the system level. In most cases, the number of transistors required for implementation of DETFFs is twice that for SETDFF's. Since dynamic flip-flops employ the capacitance of internal nodes as opposed to latches for data storage, their implementation would typically require a smaller number of transistors. Therefore, in precision applications such as SAR ADC's with a high number of bits, which require a large number of flip-flops dynamic DETFFs are preferred over their latch-based counterparts.The proposed implementation of a TSPC dynamic DETFF is shown in the block diagram of Fig. 10. This flip-flop basically consists of two TSPC dynamic SETDFFs, one of which is triggered on the rising edge (Fig. 1) and the other on the falling edge of the clock signal (Fig. 5). In the proposed topology, depending on the occurrence of the positive or the negative edge of the clock one of the two SETDFFs are selected using the 2:1 multiplexer, thereby allowing the DETFF to respond to both clock edges.

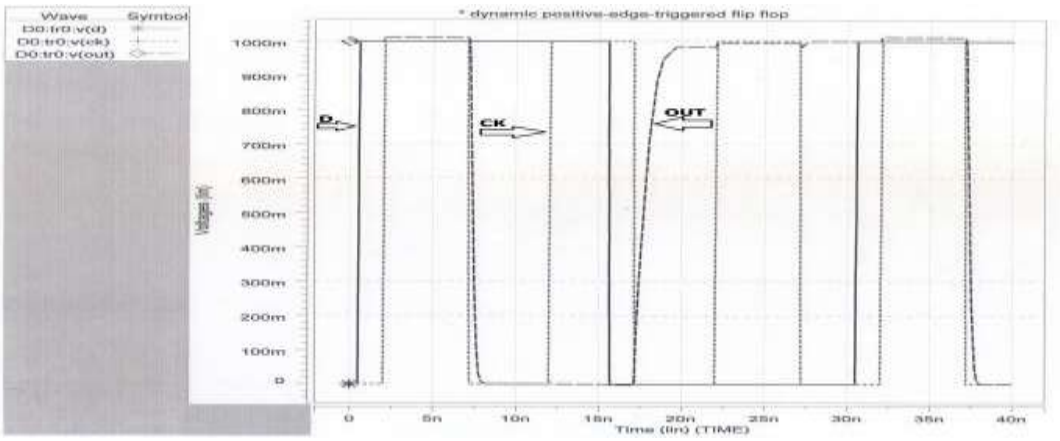


**Figure 6.** Simulated Performance of the TSPC Dynamic SETDFF of Fig. 5 in 90nm CMOS.

## 2. DISCUSSION

The slew rate of the negative clock transitions (or the clock fall times) are of consequence in the operation of the TSPC dynamic SETDFF of Fig. 1 when node N1 is to be discharged [6]. The lower the slew rate, the more charge is transported to ground during the high-to-low clock transition because both M5 and M6 will be on for $V_{out} = V_{DD}/2$, and there is an open path from N1 to ground when node N2 is high. Based on measurements, however, it was determined that the slew rate effect described herein does not affect the performance adversely for clock fall times below 10nsec in 2μm CMOS.

HSPICE simulations in a 90nm technology demonstrated that power consumption of the TSPC dynamic SETDFF was significantly lower than that of the static flip-flop using latches. As pointed out above, this can be attributed to the lower number of clocked transistors used in the TSPC topology. The TSPC SETDFF also performed slightly faster than the typical static SETDFF, as had been suggested [6], given the dynamic implementation employed in the TSPC approach.

The results of simulations on the DETFF will not be presented in this work. However, the measured performance of the TSPC positive-edge-triggered dynamic DFF in a 2μm CMOS technology and the simulated performance of a negative-edge-triggered version of the same topology designed in a 90nm technology have been presented herein. The results lend support to the feasibility of a DETFF based on the approach presented in Fig. 10. The number of transistors required for implementation of the DETFF of Fig. 10 would be less that for a static DETDFF employing latches, which would require at least twice the number of transistors as that employed in the SETDFF of Fig. 2. The DETFF based on the dynamic TSPC approach is, therefore, suitable for implementation of a compact high-resolution SAR ADC intended for biomedical implant device.

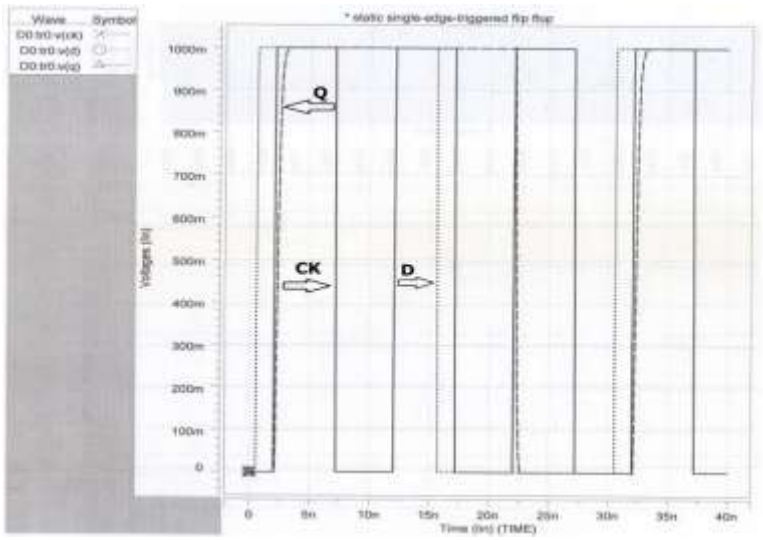


**Figure 7.** Simulated Performance of the Standard latch-based SETDFF in 90nm CMOS

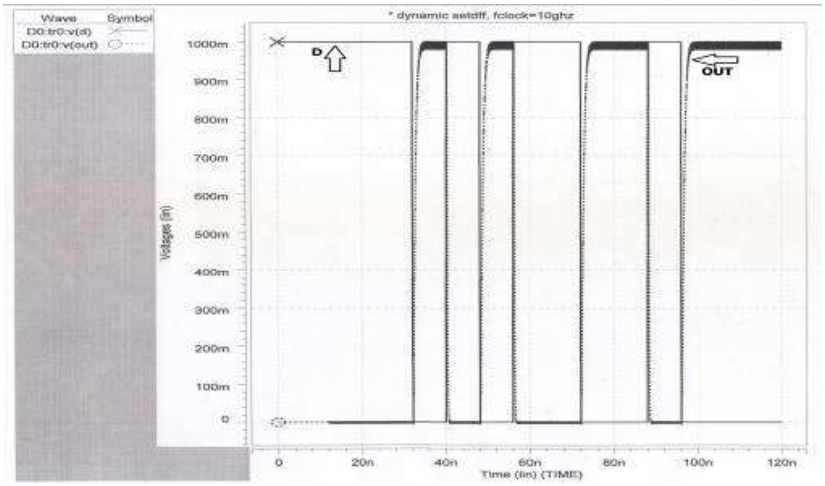


**Figure 8.** Simulated Operation of the TSPC Dynamic SETDFF in 90nm CMOS at *f*=10GHz.

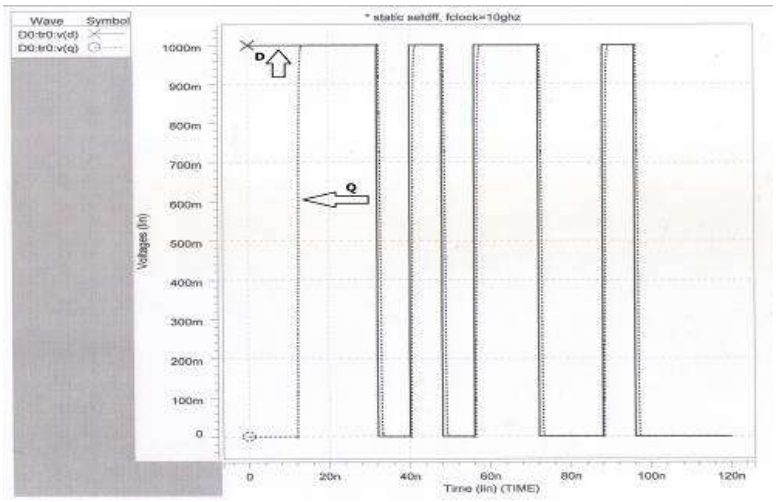


**Figure 9.** Simulated Operation of the Standard latch-based SETDFF in 90nm CMOS at *f*=10GHz

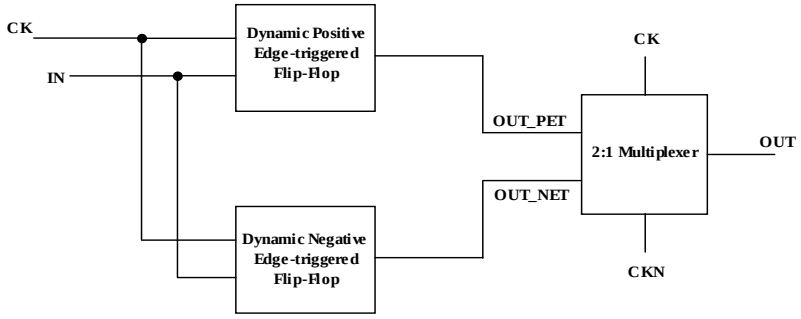


**Figure 10.** Block Diagram of the TSPC dynamic DETFF.

## 3. CONCLUSION

Compared with the static flip-flop implemented with master-slave latches, the TSPC dynamic SETDFF consumes a significantly smaller amount of power requires a smaller number of transistors and exhibits slightly shorter propagation delays. A dual-edge-triggered flip-flop topology based on the TSPC dynamic flip-flop architecture has been proposed in order to further reduce power consumption at the system level. The TSPC dynamic DETFF would require a relatively smaller number of transistors than that of a typical static DETDFF implementation based on latches.

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