International Journal of
Science and Engineering Investigations vol. 2, issue 14, March 2013
ISSN: 2251-8843

Generating Subtractor Design by QCA Gates under Nanotechnology

Bahram Dehghan
Department of Electrical Engineering, Sarvestan Branch, Islamic Azad University, Sarvestan, Iran
(bahramdehghan1@gmail.com)

Abstract- QCA is a nanotechnology that has recently been recognized as one of the top six growing technologies with potential applications in future computers. In this paper several logic gates like MV and NOT under QCA nanotechnology are presented. Boolean functions are combined by MV and NNI gates or simply NNI gates alone, eliminating inverter (NOT) gate. We described that half subtractor circuits produced by utilizing a simple recursive arrangement of 2-inputs, 2-outputs AND-NAND (A-NA) and OR-NOR (O-NO) logic gates and MV gates for full subtractor realizable with QCA (Quantum Dot Cellular Automata) technology.

We will construct the symmetric function by (EX-EXN) block which can be substituted with two (A-NA) blocks and one (O-NO) block. They can also be substituted by two (O-NO) blocks and one (A-NA) block. We will also show that if one (EX-EXN) block and (A-NA) or (O-NO) blocks are used, the output will be 1 or 0. We will also construct the half subtractor and full subtractors using QCA gates. We also indicate that by using NNI gates we can use much less NOT gates. The results show that we are able to define the above mentioned circuits with different status and same results.

Keywords- *Symmetric function, QCA gates, Subtractor design*

I. INTRODUCTION

Existing literature shows efforts to design reversible sequential circuits, but they are not based on conservative reversible logic [1].In recent years, electronic devices have seen a great improvement in the size and speed. Quantum computers are one of the most noticeable application of reversible logic. The theory of symmetric functions has found some applications in logic circuits. For example, we can produce EXOR and EXNOR gates from them that will explain in this paper.

The fundamental QCA logic primitives are the three-input majority gate, wire, and inverter. Each of these can be considered as a separate QCA locally interconnected structure, where QCA digital architectures are combinations of these cellular automata structures [2].

We believe that regular structures are good for reversible logic, because it is easier to re-use the additional outputs of reversible gates in them, instead of "wasting" them. In addition, we believe that the Linearly Independent Logic with its reversibility properties should be useful as well [3]. The basic Boolean initial in quantum cellular automata (QCA) is the majority gate. In this work, realization of half and full subtractor functions using symmetric functions and MV gates has been reported. A full subtractor is a combinational circuit that performs a subtraction between two bits, taking into account that a 1 may have been borrowed by a lower significant bit. The circuit has three inputs and two outputs that described with QCA gates in this paper.

II. QUANTUM DOT CELLULAR AUTOMATA

In order to implement a system that encodes information in the form of electron position it becomes necessary to construct a vessel in which an electron can be trapped and "counted" as it is there or not there. A quantum dot does just this by establishing a region of low potential surrounded by a ring of high potential[4].In Fig. 1 QCA cell and its binary logic are shown, the energetically position of the diagonal electrons identifies the binary logic 0 or 1. This phenomenon is useful in Nano technology which affects high resolution fast electronic circuits. In this power, consumption for changing the charge of electron is much less comparable to that of general charge carriers (hole-electron) electronic components [5].

Schematic of a basic cell is shown in Fig.1 (a). There exist two equivalent energetically minimal arrangements of the two electrons in the QCA cell, as shown in Fig.1 (b and c).

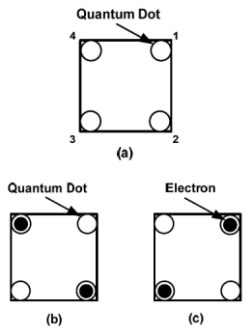

Fig1. (a) Schematic of the basic cell constructed from four quantum dots (b) P = -1(Binary 0) (c) P = +1 (Binary1)[4]

Any QCA circuit can be efficiently built using only majority gates and inverters. As shown in Fig. 2 (a), an ordinary QCA gate implementing the majority function is as follows.

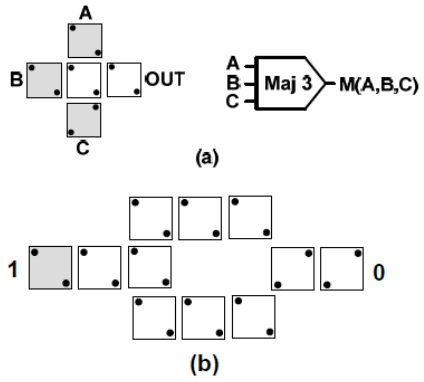

Fig2. (a) A QCA majority gate (b) A QCA inverter[4]

As illustrated in Fig. 2 (a and b), each QCA majority gate in normal form requires only five QCA cells. The QCA Majority Voter (MV) realizes MV(A, B, C) = Maj (A, B, C) = AB+BC+CA. The truth table of MV gate has been shown in table 1.

Nand-Nor-Inverter (NNI) where NNI(A, B, C) = MV(A', B, C') = A'B+BC'+C'A'. It is shown in Fig. 3. The NNI gate is a universal gate and can be employed for realizing versatile Boolean logic functions [5]. The truth table of NNI gate has been shown in table 2.

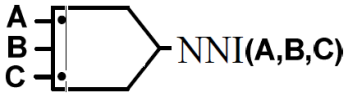

Fig. 3. QCA Nand-Nor-Inverter (NNI) Gate

A	B	C	MV(A,B,C)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

TABLE I. Truth table of MV gate

A	B	C	NNI(A,B,C)
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

TABLE II. Truth table of NNI gate

III. SYMMETRIC FUNCTION SYNTHESIS

Symmetric functions belong to the most difficult way to be realized in reversible logic. Although our circuits may look excessive to people unfamiliar with reversible logic at the first glance, their comparisons to realizations obtained by using other methods [6]. A symmetric function of n variables is one whose value at any n-tuple of arguments is the same as its value at any permutation of that n-tuple.First of all, we take 2-inputs and 2-outputs AND-NAND, OR-NOR gates as shown in Fig. 4.

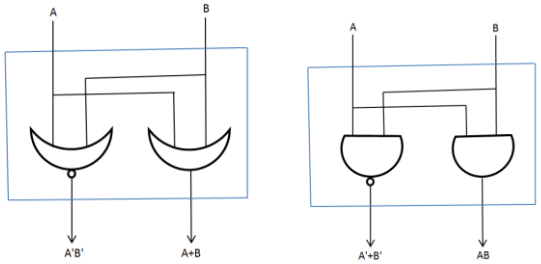

Fig. 4. 2-Inputs and 2-outputs AND-NAND Gate, 2-inputs and 2-outputs OR-NOR Gate Circuits

Here, AND-NAND gate and OR-NOR gate are two types of QCA gates which are designed on nanotechnology process. It requires less overhead area and at the same time ensures best efficiency in speed. For 2-input variables, I take one AND(A)-NAND(NA) gate and two OR(O)-NOR(NO) gates to get all the symmetric functions composed by two variables[5]. The realization of symmetric functions by AND(A)-NAND(NA) and OR(O)-NOR(NO) gates is shown in Fig. 5. Also, we can generate EXOR and EXNOR gates from 2(A-NA) and 1(O-NO) gates which are shown in Fig6. On the other hand, by replacing mentioned circuit with (EX-EXN) block we introduce some information of the circuit state and use it as a brief separated schematic. Results are shown in Fig7. Quantum computing acts an important pattern when energy efficient computations are considered.This recent scheme that can be used in related articles as producer (EX-EXN) gates widely.

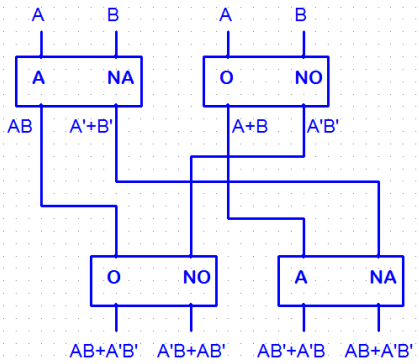

Fig.5. Symmetric functions circuit diagram for 2 input variables

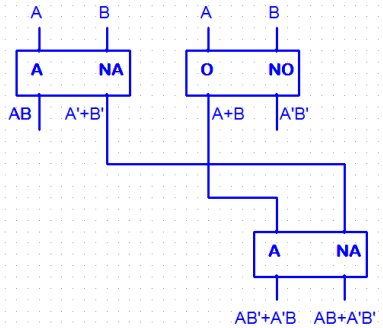

Fig.6. Symmetric functions circuit with EXOR and EXNOR outputs

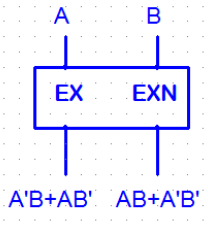

Fig.7. New equivalent circuit of Figure 6 in one block

If a block(EX-EXN) and functions(O-NO)or(A-NA) as in Fig8 is shown utilized the outputs 0 and 1 will be achieved. Similarly, results are shown in fig.9.

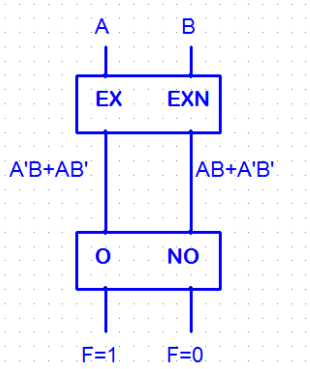

Fig.8. Using (EX-EXN) and (O-NO) to produce 1 and 0 outputs

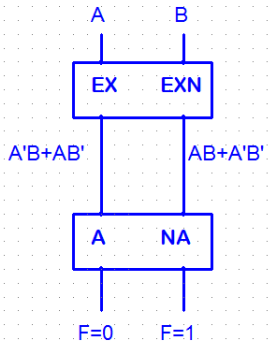

Fig.9. Using (EX-EXN) and (A-NA) to produce 0 and 1 outputs

IV. GENERATING SUBTRACTOR DESIGN BY QCA GATES

A half subtractor is an arithmetic circuit that subtracts two bits and produces their difference. The circuit has two inputs minuend (A) and subtrahend (B) and two output bits, one is the difference bit (Di) and the other is the borrow bit (Bo). The truth table of the half subtractor is axiomatic. The Boolean functions for the two outputs can be obtained directly from the truth table as:

$$\text{Difference}=A'B+AB'=A\oplus B \quad (1)$$
$$\text{Borrow}=A'B$$

Fig.10 shows symmetric functions circuit for half-subtractor. On the other hand, a full subtractoris a combinational circuit that performs a subtraction between two bits, taking into account that a 1 may have been borrowed by a lower significant bit. The circuit has three inputs and two outputs. Input variables are minuend (A), subtrahend (B), and previous borrow(C); output variables are difference (Di) and output borrow (Bo).

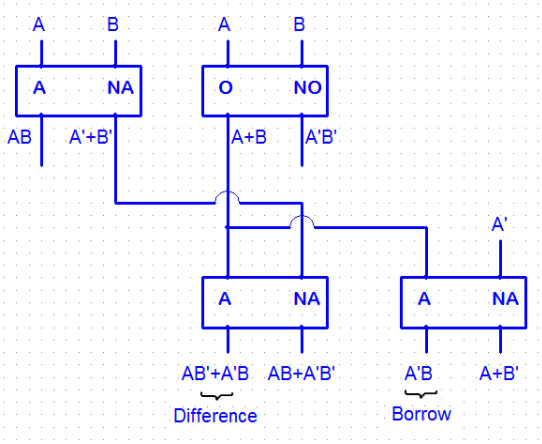

Fig.10. Symmetric functions circuit for half-subtractor

It executes the operation A – B – C. The truth table of the full subtractor is shown in table3. The simplified Boolean functions for the two outputs are:

$$Di=A\oplus B\oplus C \quad (2)$$
$$Bo=C(A\oplus B)'+A'B$$

TABLE III. Truth table of full subtractor

A	B	C	Di	Bo
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Subtraction of binary numbers is performed by taking the complement of the subtrahend and adding to the minued as the same manner in addition. It is also possible to subtract binary numbers directly using logic gates. The focuses of these structures are on introducing MV gates. However, NOT gates have been ignored in these schematics. But this way is (Majority gate reduction) easy and have less hardware requirement. Fig11 shows one design from full subtractor as a result of the following equations.

$$\text{Borrow}=MV(MV(A',B,C'),MV(A',B,C),C) \quad (3)$$
$$\text{Difference}=MV(MV(A',B,C),MV(A,B',C),C')$$

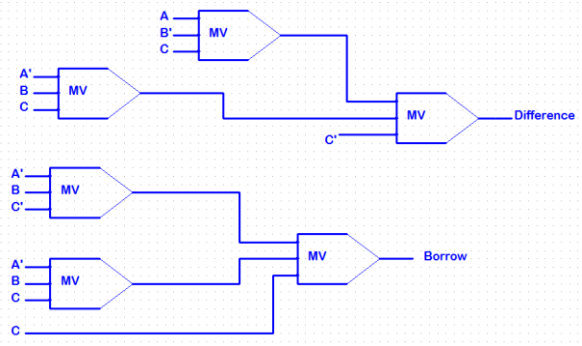

Fig.11. Full Subtractor Circuit Diagram with 5 MV gates

Also, Fig.12 shows one design from full subtractor. It is specified by the following equations.(Eq.4.)

Borrow=MV(MV(A',B,C),MV(A',B',C),B) (4)
Difference=MV(MV(A',B',C'),MV(A',B,C),A)

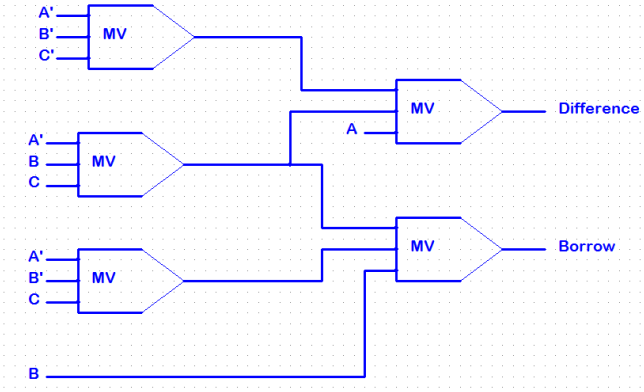

Fig.12. Full Subtractor Circuit Diagram with 5 MV gates

We can implement a full subtractor using this majority gates. As shown in Fig.13, the number of majority gates has been reduced. Majority expression of full subtractor functions operator as Eq.5.

Borrow=MV(MV(A,B',C),MV(A',B,C),B) (5)
Difference=MV(MV(A,B',C),MV(A',B,C),C')

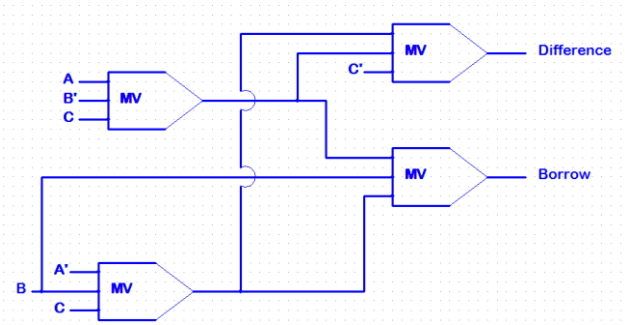

Fig.13. Full Subtractor Circuit Diagram with 4 MV gates

Similarly, the other configuration is shown in fig.14. These functions are shown in Eq. 6.

Borrow=MV(MV(A,B',C),B,A') (6)
Difference=MV(MV(A',B',C'),MV(A,B',C),B)

The above computation leads to another approach to design new structure based on MV gates.

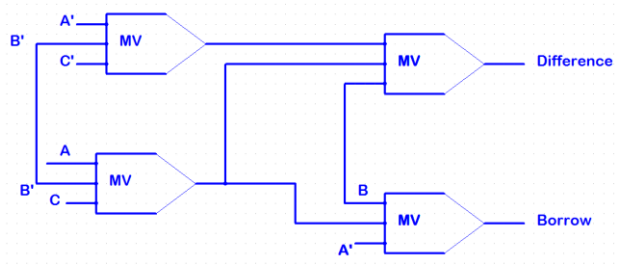

Fig.14.Full Subtractor Circuit Diagram with 4 MV gates

The characteristic equation of the NNI gate and MV gate can be written as:

NNI(A,B',C)=MV(A',B',C') (7)

In order to reduce number of NOT gates in the recent circuit, our replacement will improve results to make efficient synthesize. Hence, by replacing NNI gate in fig.14 we can produce new architecture with less NOT gates. Fig. 15. shows the proposed implementation of the Fig.14.

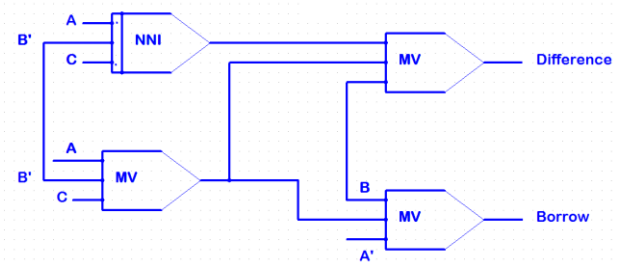

Fig.15. Full Subtractor Circuit Diagram with 3 MV and 1 NNI gates

The QCA cell is a basic building block of nanotechnology that can be used to make gates, wires and memories [7]. Results have been confirmed by the truth table. The truth table of these gates has not been shown. Because these are axiomatic, as can be seen, there are several ways to produce full subtractor using MV gates. But it is expected that the reduction MV gates in full subtractor design will eliminate significant dissipated power for future QCA architectures. All the above configuration leads to recognition of new logic circuit design which we design all the properties with QCA gates.

V. CONCLUSION

Quantum dot Cellular Automata (QCA) is one of the emerging technologies for Nano scale computation. In this paper, the operations of the half subtractor and full subtractors have been investigated according to the truth table. We had discussed the QCA technology which is becoming emerging technology in quantum computation. We had surveyed

different logic gate designs for QCA. A scheme for full subtractor has been introduced to construct a four majority gates in order to make efficient structure with mentioned output under QCA technology.The results show that any QCA circuit can be made using only majority gates and inverters. The current digital design structure purpose energy efficient realization of logic circuits and great step toward design complex logic circuits using MV gates.

REFERENCES

[1] H. Thapliyal and A. P. Vinod," Design of reversible sequential elements with feasibility of transistor implementation", Proc. ISCAS 2007, New Orleans, USA, May 2007, pp. 625-628.

[2] R. Zhang, K. Walus, Wei Wang, G.A. Jullien,"A Method of Majority Logic Reduction for Quantum Cellular Automata" IEEE Transactions on Nanotechnology, vol. 3, no. 4, December 2004.

[3] M. Perkowski, P.Kerntopf, A. Buller, M. Chrzanowska-Jeske, A. Mishchenko, X. Song, A. Al-Rabadi ,"Regularity and Symmetry as a Base for Efficient Realization of Reversible Logic Circuits", http://web.cecs.pdx.edu/~mperkows/temp/May13/tahoe5.pdf

[4] M. Rahimi Azghadi, O. Kavehei, K. Navi," A Novel Design for Quantum-dot Cellular Automata Cells and Full Adders", http://arxiv.org/ftp/arxiv/papers/1204/1204.2048.pdf

[5] P. Kanti Bhattacharjee," Digital Combinational Circuits Design with the Help of Symmetric Functions Considering Heat Dissipation by Each QCA Gate", International Journal of Computer and Electrical Engineering, Vol. 2, No. 4, August, 2010.

[6] M. Perkowski, P.Kerntopf, A. Buller, M. Chrzanowska-Jeske, A. Mishchenko, X. Song, A. Al-Rabadi, "Regular Realization of Symmetric Functions using Reversible Logic", http://web.cecs.pdx.edu/~mperkows/temp/May13/regular-reversible-perk4.pdf

[7] S. Karthigai Lakshmi , G. Athisha, "Design and Analysis of Subtractors using Nanotechnology Based QCA", European Journal of Scientific Research, Vol.53 No.4 (2011), pp.524-532