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HIGH SWING CMOS REALIZATION FOR THIRD GENERATION CURRENT CONVEYOR (CCIII)

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ABSTRACT

In this paper a new CMOS realization for third generation current conveyor (CCIII) is proposed. The proposed circuit provides high swing range at terminals X and Y. The circuit has low input impedances at terminals X and Y and high output impedance at terminals Z+ and Z-. The circuit has 180MHz -3dB cutoff frequency in voltage follower mode. SPICE simulation results using MIETEC 1.2μ CMOS process model are given.

Keywords: *CMOS Circuits, CCIII, SPICE, High swing*

1. INTRODUCTION

In 1995, third generation current conveyor (CCIII) was introduced as a new active element for conveniently taking out the current flowing through a branch of a circuit [1]. Attention was then paid to the realization of various active circuits by the use of CCIII [2-7].

The main features of the CCIII are low gain errors (high accuracy), high linearity and wide frequency response. In addition high output resistance at terminal Z of the CCIII is required to enable easy cascadability without need for additional active elements in applications. Unfortunately, because of the limited linearity and low output resistance of the basic current mirrors used in the structure of the conventional CCIII [1], its DC and AC performances are low.

In this paper, we propose a novel implementation of dual-output CCIII based on and high swing current mirrors [8]. The circuit exhibits excellent output-input gain accuracy and frequency responses. The output resistance at terminal Z+ of the proposed CCIII is calculated theoretically. Simulation results, which confirm the high performance of the proposed CCIII, are given.

2. PROPOSED CIRCUIT

The terminal relations of an ideal CCIII, which is shown in Figure 1, can be given by

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$$\begin{bmatrix} I_Y \\ V_X \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \quad (1)$$

According to this equation an ideal dual-output CCIII has a (+1) voltage gain between terminals X and Y, a (-1) current gain between terminals X and Y, a (+1) current gain between terminals X and +Z, and a (-1) current gain between terminals X and –Z. The latter property enables the use of the CCIII as an integrated floating current sensing device.

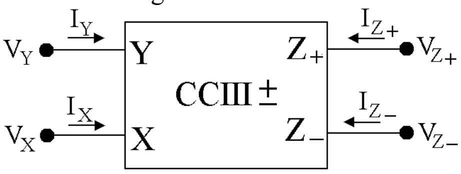

Figure 1. Electrical symbol of the CCIII.

By taking into account the deviation of the voltage and current gains from their ideal value, the defining equation of the CCIII becomes

$$\begin{bmatrix} I_Y \\ V_X \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & -\alpha & 0 & 0 \\ \beta & 0 & 0 & 0 \\ 0 & \gamma & 0 & 0 \\ 0 & -\delta & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \quad (2)$$

where α, β, γ and δ denotes the current and voltage gains which are ideally equal to unity.

The conventional third generation current conveyor is shown in Figure 2 [1]. It is based on basic current mirrors (M_6,M_8), (M_5,M_7), (M_{14},M_{16}) and (M_{13},M_{15}). The currents at terminals X and Y is transferred to the terminals Z_+ and Z_- by the output stage transistors M_{21}-M_{22} and M_{23}-M_{24}, respectively. A major advantage of this CCIII is its simple structure. The Z+ output resistance of this current conveyor is calculated as

$$R_{oz+} = (r_{ds21})//(r_{ds22}) \quad (3)$$

where r_{dsi} denotes the output resistance of the i'th MOS transistor respectively. The Z- output resistance of the conveyor can be calculated similarly. An important drawback of the conventional CCIII is the finite output resistance ($R_{oz\pm}$) and low accuracy of the voltage and current gains at terminals X and Z [9]. To increase the gain accuracy and linearity a new CCIII based on using high swing current mirror [9] in the structure of the conveyor is proposed.

The proposed high performance CCIII is shown in Figure 3. The high swing current mirrors consist of transistors (M_9-M_{12}), (M_{21}-M_{24}), (M_{13}-M_{16}) and (M_{17}-M_{20}) are used to transfer the current between terminals X and Y. The current mirrors used in the output stages of the proposed CCIII consist of transistors (M_{25}-M_{32}) and (M_{33}-M_{40}) for Z+ and (M_{41}-M_{48}) and (M_{49}-M_{56}) for Z- outputs.

Although the number of transistors used in the structure of the proposed CCIII is more than conventional and cascode one, the output resistance of this CCIII is highly increased.

The output resistance at terminal Z+ of the proposed high performance CCIII shown in Figure 3, can be calculated as:

$$R_{oz+} = [g_{m35}\, r_{ds35}\, r_{ds36}] // [g_{m34}\, r_{ds34}\, r_{ds33}] \quad (4)$$

From equation (4) one can realize that the output resistance of the proposed CCIII is much higher than conventional CCIII.

3. SIMULATION RESULTS

The performance of the proposed circuit shown in Figure 3 is verified by SPICE simulation program using 1.2 µm MIETEC CMOS process model parameters. The dimensions of the MOS transistors used for SPICE simulations are W/L=240µ/2.4µ for NMOS and W/L=720µ/2.4µ for PMOS transistors. The voltage supply used for the proposed CCIII is ±2.5 V with the bias current I_o =200µA.

The basic dc and ac characteristics such as plots of V_x against V_y, plots of V_z against V_y, frequency response of (I_z/I_x) for the proposed CCIII are obtained. The DC voltage transfer characteristic of Vx against Vy (short circuited terminal z) is shown in Figure 4. The voltage clipping limits at terminal-x are obtained as: V_{xmax}=2.3 V and V_{xmin}=-2 V. Figure 5 shows the DC current transfer characteristic of I_X-I_Y for open circuited terminal Z (R_Z=∞) and short circuited terminal X. The current clipping limits determined as: I_{xmax}=190µA and I_{xmin}=-180µA. Figure 6 shows the DC current transfer characteristic of I_{z-}-I_x for short circuited terminal Y. The current clipping limits determined as: I_{z-max}=180µA and I_{z-min}=-190µA. Figure 7 shows the DC current transfer characteristic of I_{z+}-I_x for short circuited terminal Y. The current clipping limits determined as: I_{z+max}=195μA and I_{z+min}=-180μA. The frequency response of the voltage follower (V_X/V_Y) is shown in Figure 8. The f_{-3dB} frequency is found to be 180MHz. The frequency dependencies of the impedances are shown in Figures 9-12. The X and Y input impedances of the proposed CCIII are found to be 200Ω and 1.5kΩ, respectively. The other advantage of the proposed circuit is that its output resistances at terminals Z+ and Z- are found to be 90kΩ which is 5 times larger than the output impedance of the conventional CCIII [9].

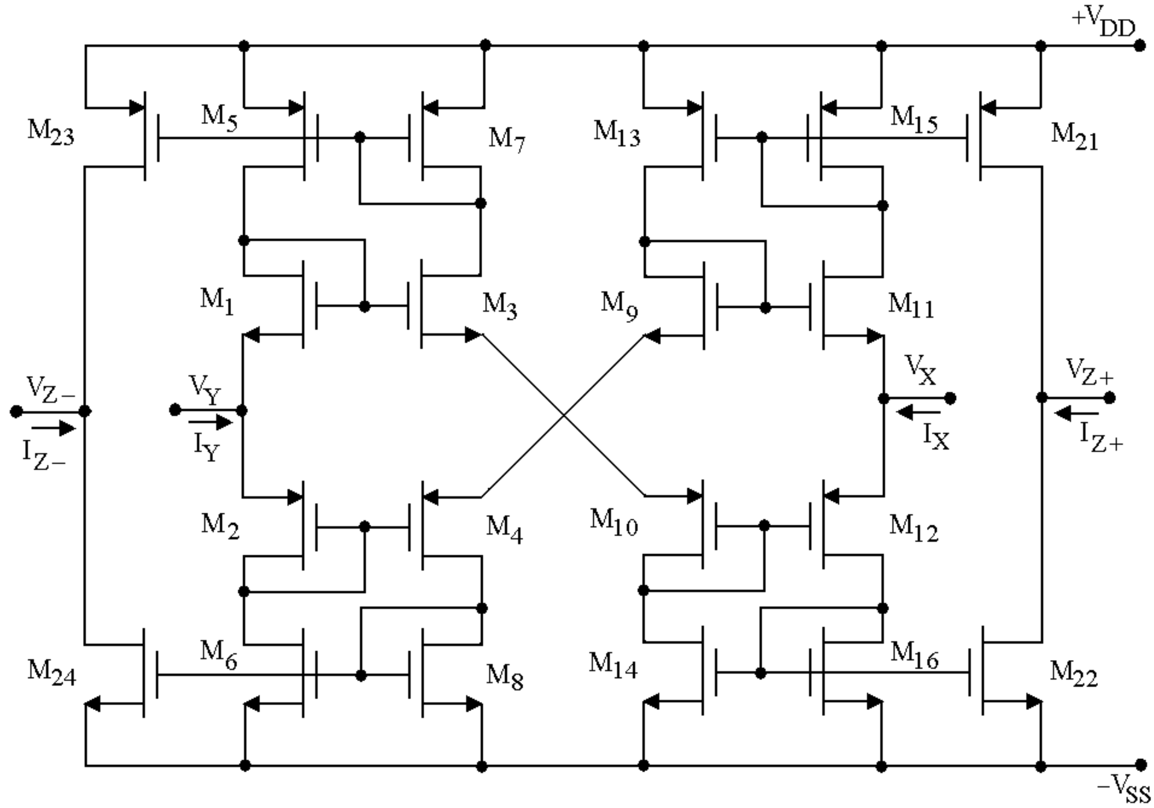

Figure 2. Conventional third generation current conveyor (CCIII).

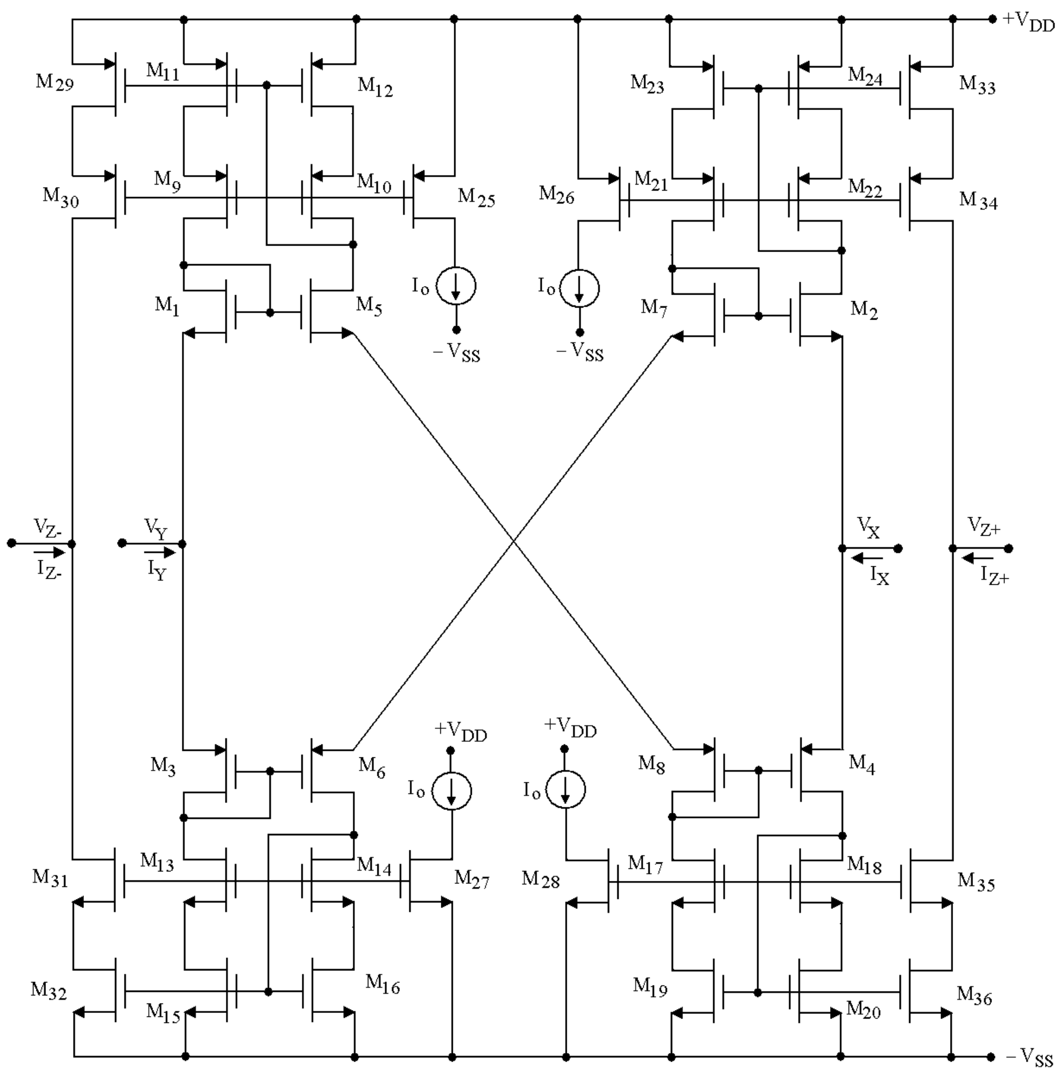

Figure 3. The proposed circuit configuration for the CCIII.

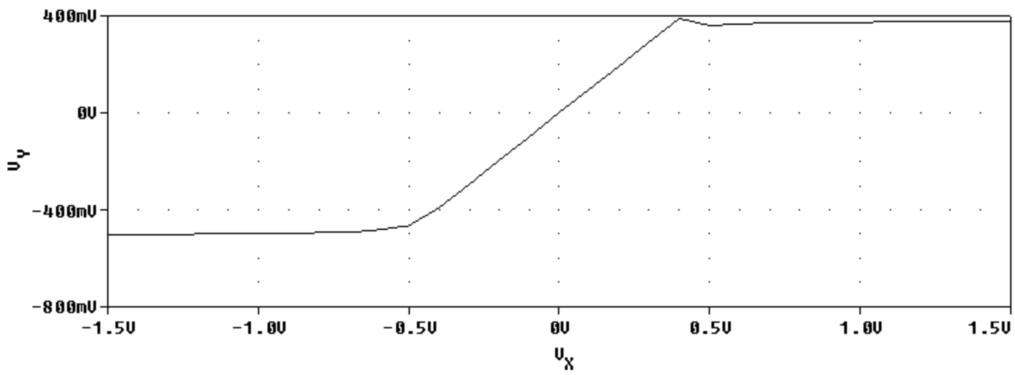

Figure 4. The characteristic of V_X-V_Y.

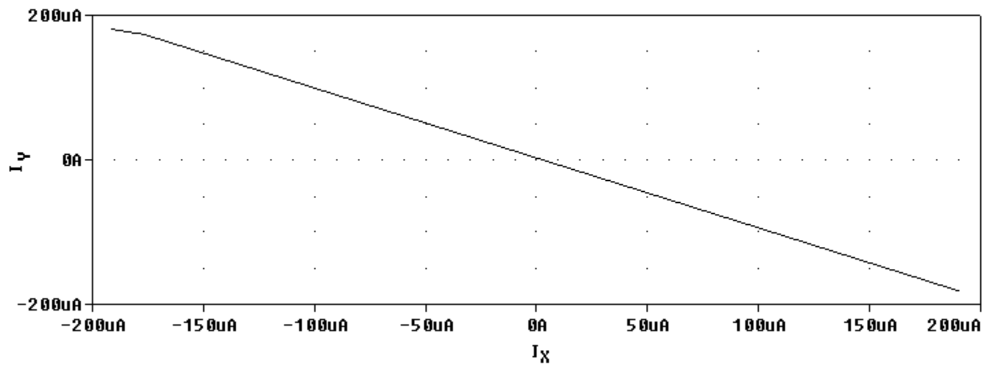

Figure 5. The characteristic of I_X-I_Y.

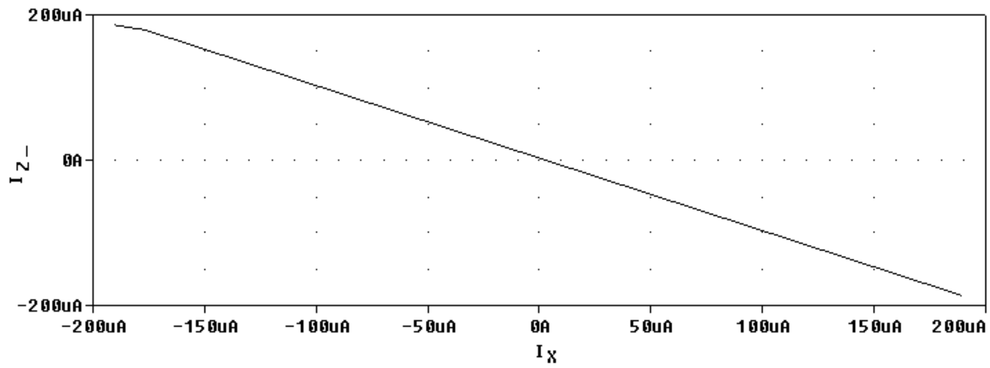

Figure 6. The characteristic of I_{z-}-I_x.

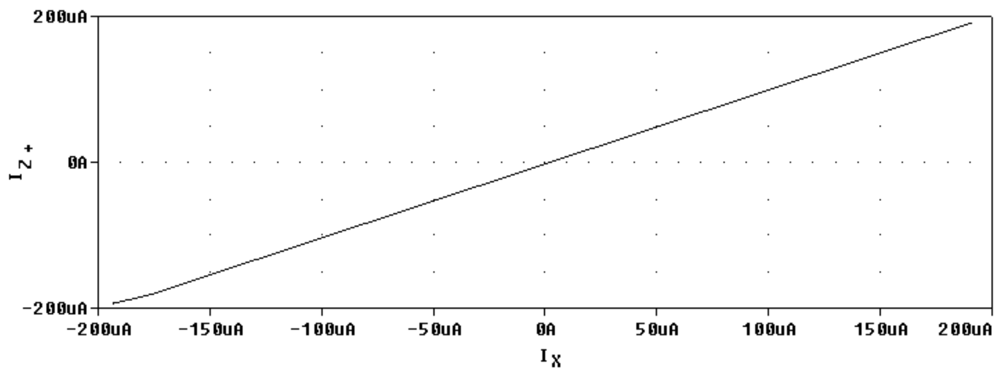

Figure 7. The characteristic of I_{z+}-I_x.

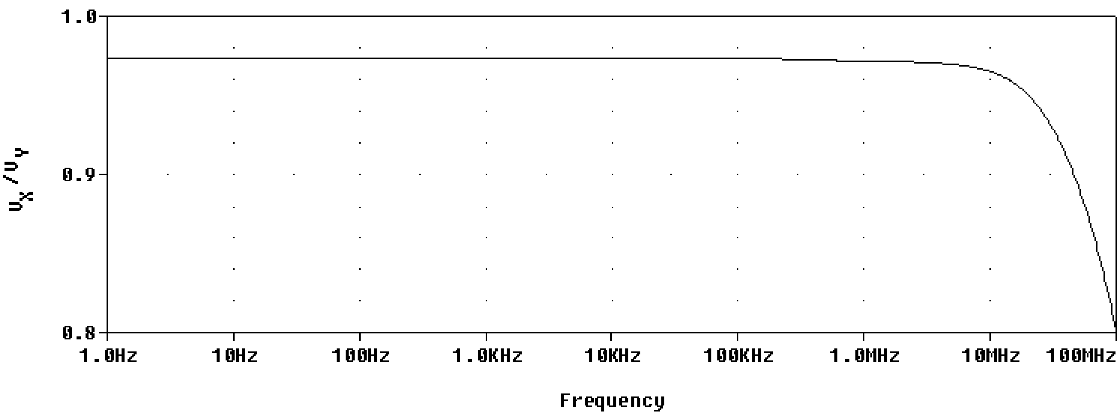

Figure 8. The characteristic of V_X/V_Y.

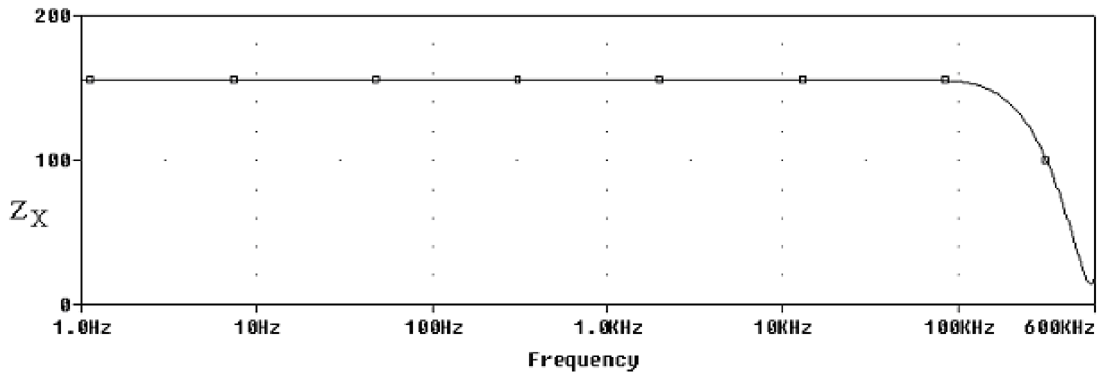

Figure 9. The frequency response of Z_X.

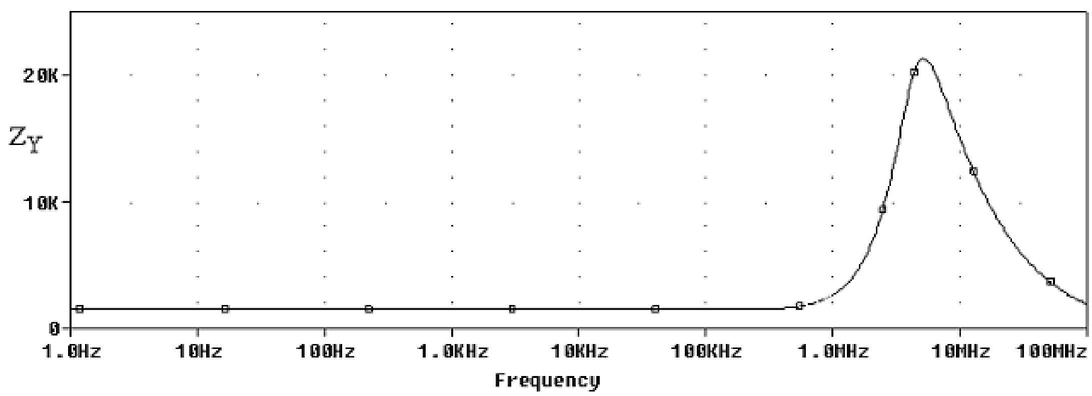

Figure 10. The frequency response of Z_Y.

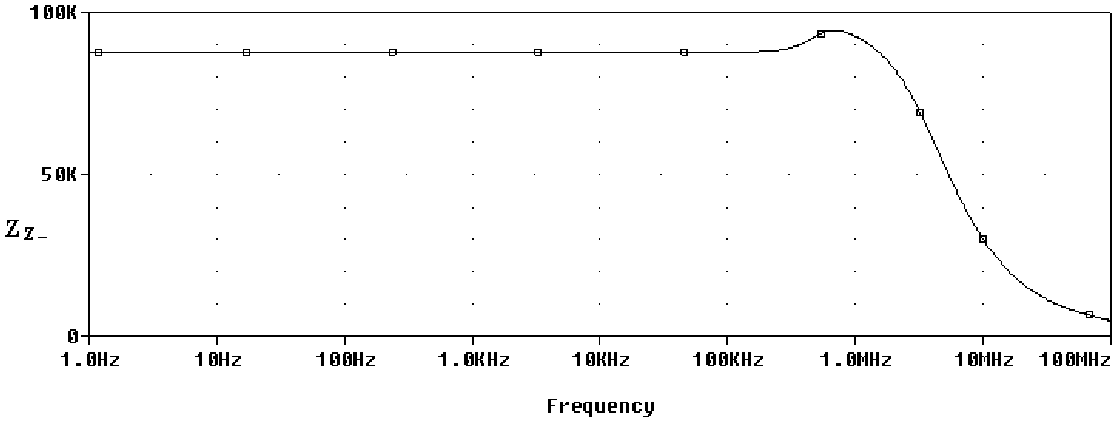

Figure 11. The frequency response of $Z_{Z\_}$.

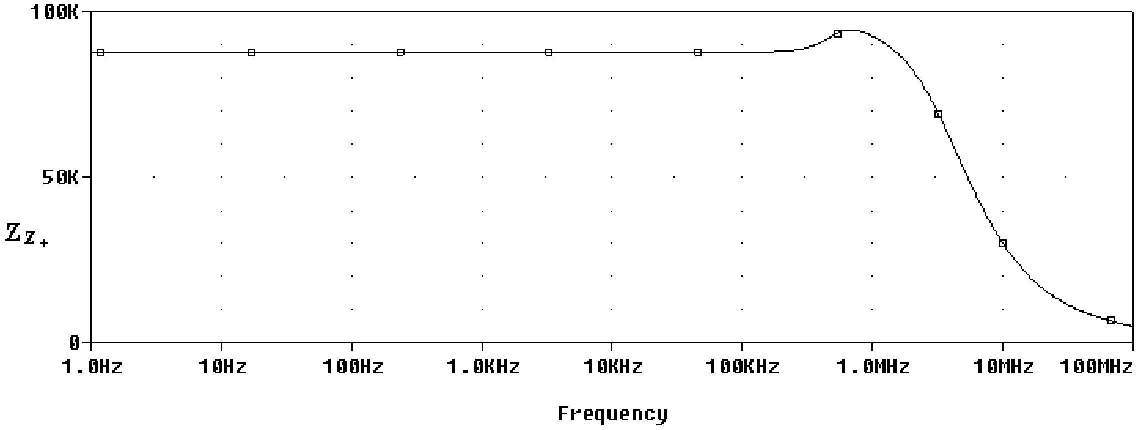

Figure 12. The frequency response of Z_{Z+}.

4. CONCLUSION

A new high performance CMOS third-generation current conveyor is presented. The proposed circuit uses high swing current mirrors, which increase accuracy of the voltage and current gains at terminals X and Z. Also the output impedance of the proposed CCIII is 5 times grater than the output impedance of conventional CCIII. The voltage frequency response of the proposed CCIII shows excellent performance. The simulation results confirm high performance of the circuits in terms of linearity, voltage and current gain accuracy.

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